rials systems originally developed at Oak Ridge National Laboratories in the 1990's, are capable of over 30,000 charge/discharge cycles without appreciable capacity fade, and can withstand intermittent heating and cooling to temperatures above 100 °C and below –40 °C.

To achieve high efficiency, the photovoltaic, thermoelectric device and the microbattery need to operate coherently. A smart power silicon chip, currently under development at JPL, will ensure the coherent operation of the energy generating and storage devices within the power tile system. This chip includes three synchronized high-efficiency DC-DC voltage converters for producing common voltage from the three sources, a battery-charging circuit, a thermoelectric heater driver circuit, and all the necessary sense and control circuits to produce the synchronized operation.

A prototype power tile, fabricated at JPL, has dimensions of 3 cm by 3 cm by 3 mm. The dual-junction photovoltaic cell in this power tile is capable of delivering a current of 125 mA at a potential of 2.1 V in full sunlight (1 AU). The thermoelectric device, a commercial off-the-shelf system 1.9 mm thick, generates a current of 20 mA at a potential of approximately 0.8 V when the photovoltaic side is at a temperature of 80 °C and the storage-battery side at a temperature of 45 °C. The battery is a 1 mm thick Li/LiPON/LiCoO solid-state multilayer system capable of delivering 20 – 50 mW of power during the 1/2 hour of ellipse time typically encountered in low Earth orbit. The photovoltaic cells and thermoelectric devices are integrated using a thermally conductive silver epoxy, while the battery is encased in aluminum. The power tile has been tested in an X-25 solar simulator and has been shown to function in a variety of conditions. Ongoing work includes miniaturizing the charge control electronics, integrating true microthermoelectric devices, and extended lifetime testing.

This work was done by Jay Whitacre, Jean-Pierre Fleurial, Mohammed Mojarradi, Travis Johnson, Margaret Amy Ryan, Ratnakumar Bugga, William West, Subbarao Surampudi, and Julian Blosiu of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1)*

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to

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Refer to NPO-30433, volume and number of this NASA Tech Briefs *issue, and the page number.*

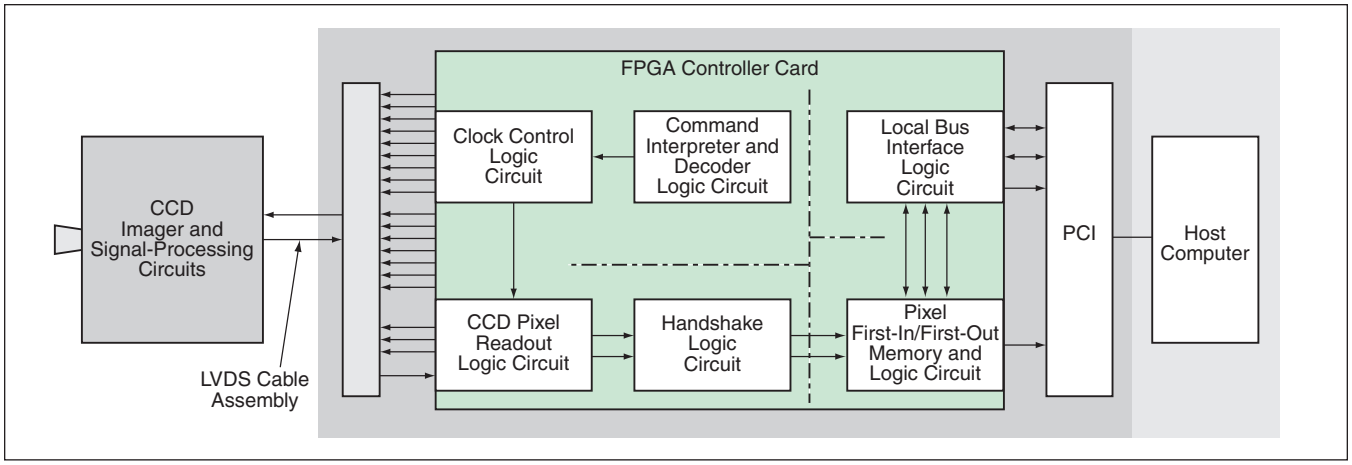
Event-Driven Random-Access-Windowing CCD Imaging System

Regions of interest can be adapted to changes in the scene.

NASA's Jet Propulsion Laboratory, Pasadena, California

A charge-coupled-device (CCD) based high-speed imaging system, called a real-time, event-driven (RARE) camera, is undergoing development. This camera is capable of readout from multiple subwindows [also known as regions of interest (ROIs)] within the CCD field of view. Both the sizes and the locations of the ROIs can be controlled in real time and can be changed at the camera frame rate. The predecessor of this camera was described in "High-Frame-Rate CCD Camera Having Subwindow Capability" (NPO-30564) *NASA Tech Briefs*, Vol. 26, No. 12 (December 2002), page 26. The architecture of the prior camera requires tight coupling between camera control logic and an external host computer that provides commands for camera operation and processes pixels from the camera. This tight coupling limits the attainable frame rate and functionality of the camera.

The design of the present camera loosens this coupling to increase the achievable frame rate and functionality. From a host computer perspective, the readout operation in the prior camera was defined on a per-line basis; in this camera, it is defined on a per-ROI basis. In addition, the camera includes internal timing circuitry. This combination of features enables real-time, event-driven operation for adaptive control of the camera. Hence, this camera is well suited for applications requiring autonomous control of multiple ROIs to track multiple targets moving throughout the CCD field of view. Additionally, by eliminating the need for control intervention by the



The **RARE Camera** is a high-speed CCD-based imaging system that offers enhanced speed and functionality for tracking moving targets.

host computer during the pixel readout, the present design reduces ROI-readout times to attain higher frame rates.

This camera (see figure) includes an imager card consisting of a commercial CCD imager and two signal-processor chips. The imager card converts transistor/transistor-logic (TTL)-level signals from a field programmable gate array (FPGA) controller card. These signals are transmitted to the imager card via a low-voltage differential signaling (LVDS) cable assembly. The FPGA controller card is connected to the host computer via a standard peripheral component interface (PCI). The host computer sends control parameters to the FPGA controller card and reads camera-status and pixel data from the FPGA controller card. Some of the operational parameters of the camera are programmable in hardware. Commands are loaded from the host computer into the FPGA controller card to define such parameters as the frame rate, integration time, and the size and location of an ROI.

There are two modes of operation: image capture and ROI readout. In image-capture mode, whole frames of pixels are repeatedly transferred from the image area to the storage area of the CCD, with timing defined by the frame rate and integration time registers loaded into the FPGA controller card. In ROI readout, the host computer sends commands to the FPGA controller specifying the size and location of an ROI in addition to the frame rate and integration time. The commands result in scrolling through unwanted lines and through unwanted pixels on lines until pixels in the ROI are reached. The host computer can adjust the sizes and locations of the ROIs within a frame period for dynamic control to changes in the image (e.g., for tracking targets).

This work was done by Steve Monacos, Angel Portillo, Gerardo Ortiz, James Alexander, Raymond Lam, and William Liu of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1)*
NPO-30878

Stroboscope Controller for Imaging Helicopter Rotors

This unit can be programmed to operate in a variety of configurations.

Ames Research Center, Moffett Field, California

A versatile electronic timing-and-control unit, denoted a rotorcraft strobe controller, has been developed for use in controlling stroboscopes, lasers, video cameras, and other instruments for capturing still images of rotating machine parts — especially helicopter rotors. This unit is designed to be compatible with a variety of sources of input shaft-angle or timing signals and to be capable of generating a variety of output signals suitable for triggering instruments characterized by different input-signal specifications. It is also designed to be flexible and reconfigurable in that it can be modified and updated through changes in its control software, without need to change its hardware.

Figure 1 is a block diagram of the rotorcraft strobe controller. The control processor is a high-density complementary metal oxide semiconductor, single-chip, 8-bit microcontroller. It is connected to a 32K × 8 nonvolatile static random-access memory (RAM) module. Also connected to the control processor is a 32K × 8 electrically programmable read-only-memory (EPROM) module, which is used to store the control software. Digital logic support circuitry is implemented in a field-programmable gate array (FPGA). A 240 × 128-dot, 40-character × 16-line liquid-crystal display (LCD) module serves as a graphical user interface; the user provides input through a 16-key keypad mounted next to the LCD. A 12-bit digital-to-analog converter (DAC) generates a 0-to-10-V ramp output signal used as part of a rotor-blade monitoring system, while the control processor generates all the appropriate strobing signals. Optocouplers are used to isolate all input and output digital signals, and optoisolators are used to isolate all analog signals.

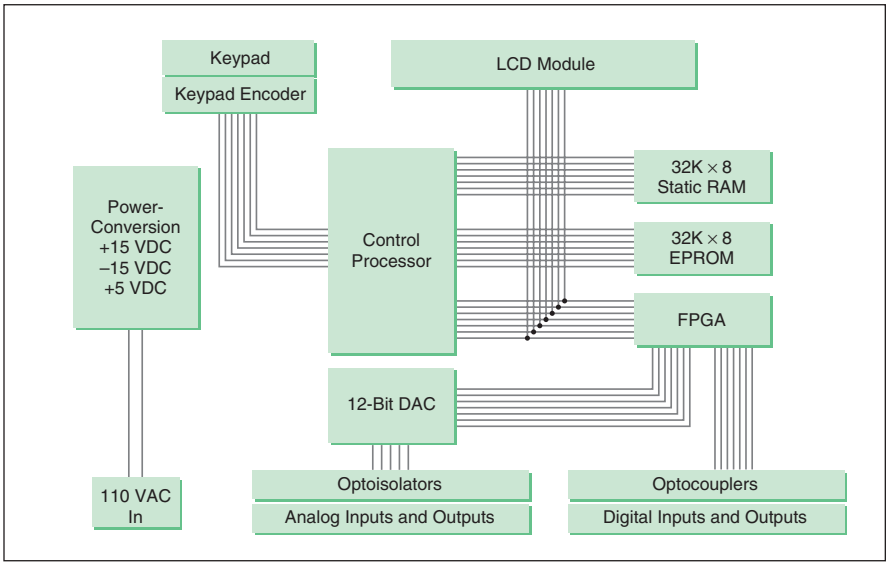


Figure 1. The **Control Processor Is Controlled by Software** that resides in the EPROM. The functionality of the system can be modified via the software, without changing the hardware.

The unit is designed to fit inside a 19-in. (≈48-cm) rack-mount enclosure. Electronic components are mounted on a custom printed-circuit board (see Figure 2). Two power-conversion modules on the printed-circuit board convert AC power to +5 VDC and ±15 VDC, respectively. Located on the back of the unit are 16 bayonet connectors used for input and output. There are 14 outputs: 10 analog voltage ramp waveforms, a once-per-revolution pulse, an *n*-times-per-revolution (where *n* is an integer selectable by the user) pulse, a transistor/transistor logic (TTL) digital strobe signal, and an open-collector digital strobe signal. There are two input connectors which accept a TTL once-per-revolution and an *n*-per-revo-