host computer during the pixel readout, the present design reduces ROI-readout times to attain higher frame rates.

This camera (see figure) includes an imager card consisting of a commercial CCD imager and two signal-processor chips. The imager card converts transistor/transistor-logic (TTL)-level signals from a field programmable gate array (FPGA) controller card. These signals are transmitted to the imager card via a low-voltage differential signaling (LVDS) cable assembly. The FPGA controller card is connected to the host computer via a standard peripheral component interface (PCI). The host computer sends control parameters to the FPGA controller card and reads camera-status and pixel data from the FPGA controller card. Some of the operational parameters of the camera are programmable in hardware. Commands are loaded from the host computer into the FPGA controller card to define such parameters as the frame rate, integration time, and the size and location of an ROI.

There are two modes of operation: image capture and ROI readout. In image-capture mode, whole frames of pixels are repeatedly transferred from the image area to the storage area of the CCD, with timing defined by the frame rate and integration time registers loaded into the FPGA controller card. In ROI readout, the host computer sends commands to the FPGA controller specifying the size and location of an ROI in addition to the frame rate and integration time. The commands result in scrolling through unwanted lines and through unwanted pixels on lines until pixels in the ROI are reached. The host computer can adjust the sizes and locations of the ROIs within a frame period for dynamic control to changes in the image (e.g., for tracking targets).

This work was done by Steve Monacos, Angel Portillo, Gerardo Ortiz, James Alexander, Raymond Lam, and William Liu of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1)*
NPO-30878

Stroboscope Controller for Imaging Helicopter Rotors

This unit can be programmed to operate in a variety of configurations.

Ames Research Center, Moffett Field, California

A versatile electronic timing-and-control unit, denoted a rotorcraft strobe controller, has been developed for use in controlling stroboscopes, lasers, video cameras, and other instruments for capturing still images of rotating machine parts — especially helicopter rotors. This unit is designed to be compatible with a variety of sources of input shaft-angle or timing signals and to be capable of generating a variety of output signals suitable for triggering instruments characterized by different input-signal specifications. It is also designed to be flexible and reconfigurable in that it can be modified and updated through changes in its control software, without need to change its hardware.

Figure 1 is a block diagram of the rotorcraft strobe controller. The control processor is a high-density complementary metal oxide semiconductor, single-chip, 8-bit microcontroller. It is connected to a 32K × 8 nonvolatile static random-access memory (RAM) module. Also connected to the control processor is a 32K × 8 electrically programmable read-only-memory (EPROM) module, which is used to store the control software. Digital logic support circuitry is implemented in a field-programmable gate array (FPGA). A 240 × 128-dot, 40-character × 16-line liquid-crystal display (LCD) module serves as a graphical user interface; the user provides input through a 16-key keypad mounted next to the LCD. A 12-bit digital-to-analog converter (DAC) generates a 0-to-10-V ramp output signal used as part of a rotor-blade monitoring system, while the control processor generates all the appropriate strobing signals. Optocouplers are used to isolate all input and output digital signals, and optoisolators are used to isolate all analog signals.

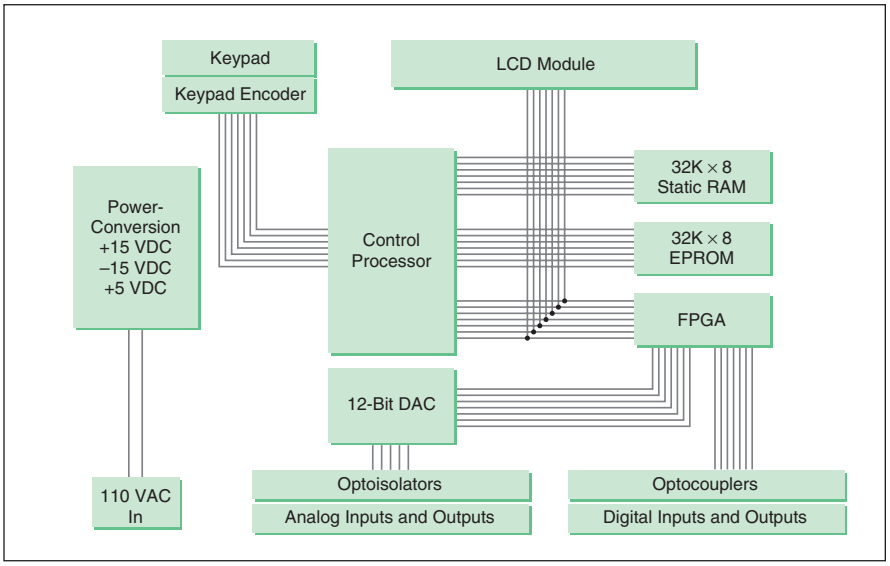

Figure 1. The **Control Processor Is Controlled by Software** that resides in the EPROM. The functionality of the system can be modified via the software, without changing the hardware.

The unit is designed to fit inside a 19-in. (≈48-cm) rack-mount enclosure. Electronic components are mounted on a custom printed-circuit board (see Figure 2). Two power-conversion modules on the printed-circuit board convert AC power to +5 VDC and ±15 VDC, respectively. Located on the back of the unit are 16 bayonet connectors used for input and output. There are 14 outputs: 10 analog voltage ramp waveforms, a once-per-revolution pulse, an *n*-times-per-revolution (where *n* is an integer selectable by the user) pulse, a transistor/transistor logic (TTL) digital strobe signal, and an open-collector digital strobe signal. There are two input connectors which accept a TTL once-per-revolution and an *n*-per-revo-

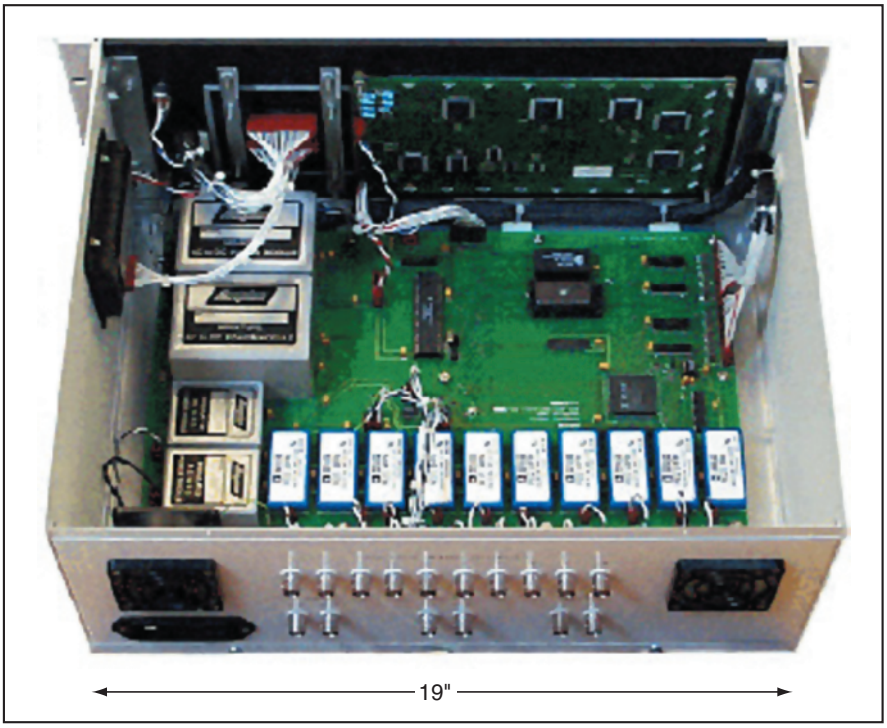

Figure 2. The **Rack-Mount Enclosure** was photographed from above and behind with the cover removed to show components mounted on the printed-circuit board.

lution signal. They can be either single-ended, floating, or differential.

The control software was written in the C language. The main functions of the software are to read data present on the control-processor ports, generate the strobe signals, generate the ramp information used to monitor rotor-blade parameters by writing to the 12-bit DAC, save and retrieve configuration settings to and from the nonvolatile RAM, communicate with the FPGA, accept keypad input, and control and update the LCD by paging though appropriate user selections and menus. The user can gain access to several menus to set such parameters as the number of blades to track, the blade-offset angle, and the number of pulses per revolution.

This work was completed for Jon Lautenschlager of the U.S. Army Aviation and Missile Command by Scott Jensen, John Marmie, and Nghia Mai of **Ames Research Center**. *Further information is contained in a TSP (see page 1)*

Inquiries concerning rights for the commercial use of this invention should be addressed to the Patent Counsel, Ames Research Center, (650) 604-5104. Refer to ARC-14966.