

of locations is optimal in the sense that it yields an optimal combination of gains, matched 3-dB widths, low cross-polarization, and low side-lobe levels. The elliptical shape of the scanning mirror was cho-

sen, from among a number of superquadric shapes, as the one that results in the lowest overall side-lobe levels.

This work was done by Ziad A. Hussein of Caltech and Ken Green of Microwave Engi-

neering Corp. for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-30506

Eight-Channel Continuous Timer

This timer measures every cycle of every input clock signal.

NASA's Jet Propulsion Laboratory, Pasadena, California

A custom laboratory electronic timer circuit measures the durations of successive cycles of nominally highly stable input clock signals in as many as eight channels, for the purpose of statistically quantifying the small instabilities of these signals. The measurement data generated by this timer are sent to a personal computer running software that integrates the measurements to form a phase residual for each channel and uses the phase residuals to compute Allan variances for each channel. (The Allan variance is a standard statistical measure of instability of a clock signal.) Like other laboratory clock-cycle-measuring circuits, this timer utilizes an externally generated reference clock signal having a known frequency (100 MHz) much higher than the frequencies of the input clock signals (between 100 and 120 Hz). It counts the number of reference-clock cycles that occur between successive rising edges

of each input clock signal of interest, thereby affording a measurement of the input clock-signal period to within the duration (10 ns) of one reference clock cycle. Unlike typical prior laboratory clock-cycle-measuring circuits, this timer does not skip some cycles of the input clock signals. The non-cycle-skipping feature is an important advantage because in applications that involve integration of measurements over long times for characterizing nominally highly stable clock signals, skipping cycles can degrade accuracy.

The timer includes a field-programmable gate array that functions as a 20-bit counter running at the reference clock rate of 100 MHz. The timer also includes eight 20-bit latching circuits — one for each channel — at the output terminals of the counter. Each transition of an input signal from low to high causes the corresponding latching circuit to latch

the count at that instant. Each such transition also sets a status flip-flop circuit to indicate the presence of the latched count. A microcontroller reads the values of all eight status flip-flops and then reads the latched count for each channel for which the flip-flop indicates the presence of a count. Reading the count for each channel automatically causes the flip-flop of that channel to be reset. The microcontroller places the counts in time order, identifies the channel number for each count, and transmits these data to the personal computer.

This work was done by Steven Cole of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

The software used in this innovation is available for commercial licensing. Please contact Don Hart of the California Institute of Technology at (818) 393-3425. Refer to NPO-40233.

Reduction of Phase Ambiguity in an Offset-QPSK Receiver

Ambiguity would be reduced to twofold at no cost in power efficiency.

NASA's Jet Propulsion Laboratory, Pasadena, California

Proposed modifications of an offset-quadrature-phase-shift keying (offset-QPSK) transmitter and receiver would reduce the amount of signal processing that must be done in the receiver to resolve the QPSK fourfold phase ambiguity. Resolution of the phase ambiguity is necessary in order to synchronize, with the received carrier signal, the signal generated by a local oscillator in a carrier-tracking loop in the receiver. Without resolution of the fourfold phase ambiguity, the loop could lock to any of four possible phase points, only one of which has the proper phase relationship with the carrier.

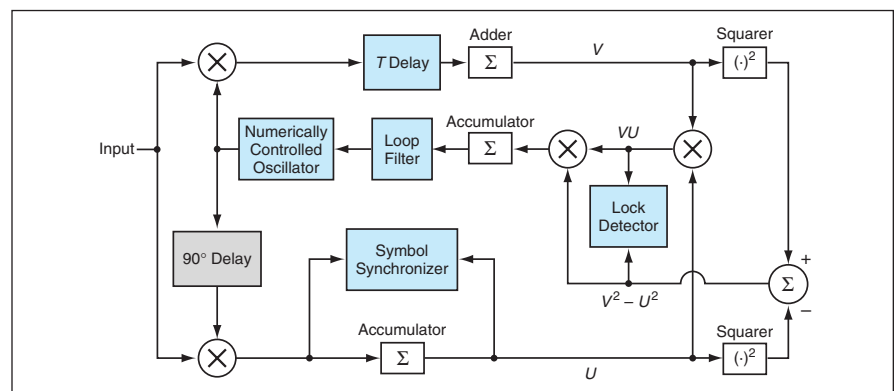


Figure 1. This **Carrier-Tracking Loop** of an offset-QPSK receiver differs from a maximum a posteriori (MAP) carrier-tracking loop of a non-offset-QPSK receiver by incorporating a unit that imposes a delay of one symbol period (T).