Fabrication of Channels for Nanobiotechnological Devices

Nanolithography would not be necessary for establishing channel depths and thicknesses.

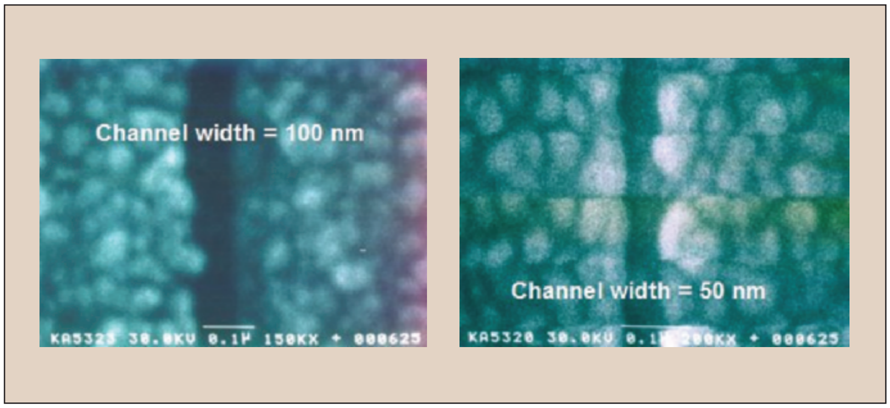
NASA's Jet Propulsion Laboratory, Pasadena, California

A method, now undergoing development, of forming nanochannels in planar substrates is intended to enable the fabrication of advanced fluidic devices that could be integrated with complementary metal oxide semiconductor (CMOS) electronic circuits. Such integral combinations of fluidic and electronic components ("laboratory-on-a-chip" devices) could be used, for example, to detect individual molecules of deoxyribonucleic acid (DNA) and proteins. The width of a channel in such a device would be chosen so that molecules of the species of interest would move along the channel in single file.

In addition to being intended to enable the tailoring of the width of each channel to a uniform value of the order of several nanometers, the developmental method is intended to satisfy the following other requirements:

- A channel must be optically transparent when viewed along a line perpendicular to the plane of the substrate;
- The process of formation of the channels must be compatible with CMOS circuitry and with the processes of fabrication of CMOS circuitry;
- Relative to processes that have been used to fabricate devices containing microchannels, this process must be simple.

In this method, the fabrication of channels includes the use of such CMOS-compatible processes as chemical-mechanical polishing and oxide deposition. The layout of the channels in the substrate plane is determined by a single photolithographic process, but it is not a nanoscale lithographic process, and this process is not relied upon to define the thickness and width of the channels. Stating it from a slightly different perspective, unlike in the prior fabrication of electronic and fluidic devices involving the use of lithography to define microscale features, this process does not include the use of lithography to define nanoscale features. It is this aspect of the method that enables simplification of the process and, hence, a decrease in cost.



These **Scanning Electron Micrographs** show channels of two different widths that were fabricated by the present method. In a finished device, the channels would be covered with an SiO_2 membrane, which would be sufficiently transparent to enable analysis of specimens in the channels by use of a fluorescence microscope.

A typical fabrication process according to this method includes, among other things, thermal oxidation to form a layer of SiO_2 on a silicon substrate, followed by deposition of a layer of Si_3N_4, followed by deposition of a first layer of polycrystalline silicon (poly-Si). The depth of the channel(s) is determined by the thickness of the first poly-Si layer. The width of the channels (see figure) is determined by the thickness of the SiO_2 layer, which thickness is readily controllable and can be made extremely uniform.

This work was done by Choonsup Lee and Eui-Hyeok Yang of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*

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Improved Thin, Flexible Heat Pipes

Like common tapes, these heat pipes can be adhesively bonded to curved objects.

Lyndon B. Johnson Space Center, Houston, Texas

Flexible heat pipes of an improved type are fabricated as layers of different materials laminated together into vacuum-tight sheets or tapes. In comparison with prior flexible heat pipes, these flexible heat pipes are less susceptible to leakage. Other advantages of these flexible heat pipes, relative to prior flexible heat pipes, include high reliability and greater ease and lower cost of fabrication. Because these heat pipes are very thin, they are highly flexible. When coated on outside surfaces with adhesives, these flexible heat pipes can be applied, like common adhesive tapes, to the surfaces of