11.6

A Radiation Hard Multi-Channel Digitizer ASIC for Operation in the Harsh Jovian Environment

S. Aslam[1], A. Akturk[2], G. Quilligan[3]

[1]NASA, Goddard Space Flight Center, Planetary Systems Laboratory, Greenbelt Road, MD, 20771, USA

[2]CoolCAD Electronics, LLC, 5000 College Avenue, Suite 2103, College Park, MD 20740, USA

[3]NASA, Goddard Space Flight Center, Instrumentation Electronics Development Branch, Greenbelt, MD 20771

11.6.1 Introduction

In 1995, the Galileo spacecraft [1][2] arrived at Jupiter to conduct follow-up experiments on pathfinder Pioneer [3][4] and key Voyager [5][6][7] discoveries especially at Io, Europa, Ganymede and Callisto [8]. These new observations helped expand our scientific knowledge of the prominent Galilean satellites; studies revealed diversity with respect to their geology, internal structure, evolution and degree of past and present activity [2][8][9]. Jupiter's diverse Galilean satellites, of which three are believed to harbor internal oceans, are central to understanding the habitability of icy worlds. Galileo provided for the first time compelling evidence of a near-surface global ocean on Europa [10][11][12][13]. Furthermore, by understanding the Jupiter system and unraveling the history of its evolution from initial formation to the emergence of possible habitats and life, gives insight into how giant planets and their satellite systems form and evolve [14]. Most important, new light is

shed on the potential for the emergence and existence of life in icy satellite oceans [15]. In 2009, NASA released a detailed Jupiter Europa Mission Study (EJSM) [16] that proposed an ambitious Flagship Mission to understand more fully the satellites Europa [11] and Ganymede [14] within the context of the Jovian system. Key to EJSM is the NASA led Jupiter Europa Orbiter (JEO) [17] and the ESA led Jupiter Ganymede Orbiter (JGO) [18]. JEO and JGO would execute a choreographed exploration of the Jovian system before settling into orbit around Europa and Ganymede, respectively. The National Academies Planetary Decadal Survey, 2011 [19] has listed the NASA-led JEO as the second highest priority mission for the decade 2013-2022, and if chosen it would be launched in 2020 with arrival at Jupiter in 2025. If the JEO mission is not chosen it is anticipated that there will be opportunities in future decadal cycles. Jupiter Orbit Insertion (JOI) begins a 30-month Jovian system tour followed by nine months of science mapping after Europa Orbit Insertion (EOI) in July 2028. The orbiter will

ultimately impact the surface of Europa after the mission is completed. The current JEO mission concept includes a range of instruments on the payload, to monitor dynamic phenomena (such as Ios volcanoes and Jupiters atmosphere), map the Jovian magnetosphere and its interactions with the Galilean satellites, and characterize water oceans beneath the ice shells of Europa and Ganymede [15][17]. The payload includes a low mass (3.7 Kg) and low power (< 5 W) Thermal Instrument (TI) concept for measuring possible warm thermal anomalies on Europa's cold surface caused by recent (< 10,000 years) eruptive activity [20][21]. Regions of anomalously high heat flow will be identified by thermal mapping using a nadir pointing, push-broom filter radiometer that provides far-IR imagery in two broad band spectral wavelength regions, 8-20 μm and 20-100 μm, for surface temperature measurements with better than a 2 K accuracy and a spatial resolution of 250 m/pixel obtained from a 100 Km orbit. The temperature accuracy permits a search for elevated temperatures when combined with albedo information. The spatial

resolution is sufficient to resolve Europa's larger cracks and ridge axial valleys. In order to accomplish the thermal mapping, the TI uses sensitive thermopile arrays that are readout by a custom designed low-noise Multi-Channel Digitizer (MCD) ASIC that resides very close to the thermopile linear array outputs. Both the thermopile array and the MCD ASIC will need to show full functionality within the harsh Jovian radiation environment, operating at cryogenic temperatures, typically 150 K to 170 K. In the following, a radiation mitigation strategy together with a low risk Radiation-Hardened-By-Design (RHBD) methodology [22] using commercial foundry processes is given for the design and manufacture of a MCD ASIC that will meet this challenge.

11.6.2 Jovian Radiation Environment

Jupiter has a strong magnetosphere [23][24][25][26] that has

led to the formation of trapped radiation belts [27][28]. Jupiter is approximately eleven times the size of the Earth, it's equatorial magnetic field strength is about 0.428 mT which is ten times stronger than Earth's and corresponds to a dipole magnetic moment of about 1.53×10^{20} Tm^3 nearly eighteen thousand times stronger than Earth's [29]. The Jovian satellites of interest and in particular Europa lie well within the radiation belt. For the planned JEO mission, the spacecraft would be irradiated by four major radiation sources [30][31]. During the interplanetary cruise phase, instrumentation will be subjected to (i) solar energetic particles consisting of protons, electrons and heavy ions, and (ii) galactic cosmic rays (protons and heavy ions). During gravity assists in the inner Jupiter system after JOI to shape the trajectory for EOI and then for the remaining 9-month mission to map out Europa, instrumentation will be subjected to (iii) intensely high-energy trapped electrons, protons and heavy ions. Finally, instrumentation will be subjected to (iv) energetic neutron and gamma particles from the onboard nuclear power source,

a Multi-Mission Radioactive Thermal Generator (MMRTG). The release of various atomic elements from the volcanic action on Io also adds to the particle densities, compounding the problem within the belts. The resulting high-energy trapped electrons and protons in the Jovian magnetosphere are the dominating sources for the significant life-limiting cumulative radiation dose both in terms of Total Ionizing Dose (TID) and Displacement Damage Dose (DDD). The Jovian trapped particles are not static, but vary in intensity and population spatially and temporally. A semi-empirical Jovian radiation environment model, based on the original Divine [32] and GIRE [33][34] models, augmented with Galileo Energetic Particle Detector (EPD) [35] and Heavy Ion Counter (HIC) [36] data together with a revised VIP4 B-field model [24] indicates that elevated radiation levels (e.g., from solar events) can be intense, but are short lived, lasting on the order of days at a time. Therefore, with allowance for spatial variation, the statistical average dose provides a reasonable estimate of radiation exposure over the mission life-

time. For some radiation effects, the momentary flux, rather than the accumulation, is of concern, e.g., flux dependent noise in sensors. Here, temporal variations are significant but the same models that justify averaging of cumulative effects from the background flux also provide insight into the intensity and duration of the flux peaks. The radiation models also indicate that Europa casts a radiation shadow [37], thereby substantially reducing radiation on one side as it orbits Jupiter. Consequently, while the spacecraft is in orbit about Europa it will spend about half its time well within the shadow, JEO would accumulate on average radiation effects at a substantially lower rate. However, the updated GIRE model still gives very high levels of integrated electron and proton fluence over a wide energy range, see Figure 11.6.1. From the resulting fluxes, 3D radiation transport code [38][39] is used to estimate the dose-depth curve for the mission, see Figure 11.6.2. For the JEO mission, a reference radiation design point of 2.9 Mrad (Si) TID behind 2.54 mm (100-mil) thick aluminum shielding with an engineering Radiation Design

Factor (RDF) of 1 [40] is chosen. This level is unprecedented and is seven times greater than any previous NASA mission to date.

11.6.3 Radiometry Application

To map surface temperature anomalies and thermal inertia of a cold moon like Europa, from a spaceborne platform, relies on accurately measuring the infrared spectral radiance [41]. One sensitive measurement technique employs a filter radiometer operating in the nadir pointing, push-broom mode that uses several thermopile linear arrays, with each array integrated to infra-red filters that have appropriate wavelength pass bands [42]. The thermopile pixels are readout with a custom built MCD ASIC. The ASIC will include a high-resolution multi-channel Analog-to-Digital Converter (ADC) that needs to operate under the extremely high levels

of radiation as described earlier in § 11.6.2 as well as at relatively low temperatures in the 150 K to 170 K range: the expected temperature range of the instrument housing in thermal equilibrium with its space environment.

11.6.3.1 Thermopile Arrays

Thermopiles based on Bi-Sb thermoelectric materials [43][44] are thermal detectors of choice for long duration planetary missions [41] because they (i) generate an output voltage that is proportional to the incoming radiation within the spectral range being mapped; (ii) do not require an electrical bias or an optical chopper; (iii) have negligible 1/f noise, (iv) do not require active cooling and (v) show radiation hardness to 10 Mrad (Si) TID [45]. Furthermore, Bi-Sb thermoelectric materials show better efficiency in the range 150 K to 200 K [46]. The TI observation cycle consists of 110 ms signal integration intervals, interspersed with instrument views of an internal blackbody. This corresponds to a 10 Hz frequency range. Thus low 1/f noise in both the detec-

tors and the readout circuitry is essential. Thermopile detectors intrinsically have low 1/f noise because when read out with high-input-impedance voltage amplifiers they exhibit negligible current flow. Thermopile elements have a typical electrical resistance of 9 kΩ and are therefore dominated by Johnson noise, i.e. 9 nV/√Hz. With a 9 kΩ source resistance, the MCD ASIC has an input-referred noise of 14.5 nV/√Hz for 10Hz. Thus the readout chip is the dominant focal plane noise source. Even with this readout noise, the TI thermopiles demonstrate a specific detectivity, D*, value of 10^9 (cm√Hz)/W for 10 Hz.

11.6.3.2 MCD ASIC

The thermopile pixels are read out in parallel with a custom MCD ASIC comprising signal conditioning, modulation, gain, multiplexing, demodulation and 16-bit digitization functions. The roughly dc signal from each pixel is modulated by an electronic chopping circuit. The resulting AC signal is amplified, demodulated, integrated and digitized. Be-

cause amplification occurs at a high frequency rather than near dc, the 1/f noise in the CMOS amplifier is dramatically reduced. Integrated signals of each of the thermopile channel outputs are multiplexed into a single analog output stream. Mounted on the same substrate as the thermopile arrays are thermistors that monitor any temperature drift of the arrays on the focal plane assembly. The pixel and thermistor outputs connect directly to the MCD ASIC that amplifies, integrates and digitizes the signals. Since the thermopile array can have as many as 64-pixels, the readout needs to be a multi-channel implementation. The MCD, illustrated as part of a simplified application in Figure 11.6.4 for a 64-pixel linear array, has 16 thermopile pixel readout channels and one temperature sensor channel. Four such ASICs interface to the array and are in close proximity so as to minimize noise pick-up and parasitic thermocouple effects. One consequence of this placement is each MCD must operate in a cryogenic environment where the ambient temperature is as low as 150 K, far below the temperatures at which commer-

cial grade chips operate at, i.e. 248 K. Cryogenic ambients also impact on the radiation hardness of the MOS devices: TID induced positive charge captured in the gate oxide increases with falling temperature that does not anneal with time or bias [47].

In addition to meeting demanding electrical specifications, the design of the TI concept places a heavy emphasis on minimizing mass, volume, and power dissipation (MVP) while maximizing longevity in Jupiter's harsh environment awash with high energy particles. Minimizing the MVP is vital to the pragmatic needs of constraining launch cost, which limits the fuel needed for the trip to Jupiter and ultimately the size of the MMRTG. In addition to ensuring that a circuit will work reliably over the mission lifetime in an extreme environment, RHBD figures very prominently in the MVP product: if a circuit can be radiation hardened, there is less of a shielding requirement which reduces the mass of the instrument significantly.

11.6.4 Radiation Mitigation Strategy

If the MCD ASIC is not designed to be sufficiently radiation hard or adequately shielded [22][48] it will be vulnerable to failure when exposed to the high radiation environment within the Jovian magnetosphere. Mission assurance and risk mitigation requirements will require that any ASIC used will have been designed and verified with the most robust, thorough, and effective process possible in order to withstand the radiation levels encountered during the mission lifetime of 10 years. The baseline JEO electronic subsystem design includes a 6U shielded chassis to reduce the radiation dose to one half the part level tolerance value (RDF = 2) to house and protect electronics. The RDF provides a systematic approach to managing the risk posed by uncertainties in both the radiation model and the ASIC radiation tolerance. For example, if there are 300 krad (Si) parts used in the electronics, the RDF = 2 designed 6U shielded chassis brings the TID down to 150

krad (Si). The MCD ASIC readout needs to be mounted very close to the linear thermopile arrays because of the low thermopile voltage outputs [49] expected and noise pickup considerations. The ASIC will therefore require spot shielding that meets the imposed JEO mission RDF = 3 requirement. A commercially available ASIC that is radiation hard to 300 krad (Si) would need to be spot shielded with an enclosure that has 25.4 mm (1000 mils) thick aluminum walls. For an enclosure volume to adequately house the MCD ASIC mounted on a ceramic board with signal conditioning components would represent a large mass penalty, clearly for a low mass TI concept this is unviable. In order to reduce the spot shielding mass significantly, a custom radiation hard MCD ASIC tolerant to at least 3 Mrad (Si) TID is required. For the same enclosure volume, the resulting aluminum shielding thickness would be significantly reduced giving nearly a 10-fold reduction in shielding mass. Currently, an effort is being made to fabricate a 32-channel radiation hard ASIC for thermopile readout at Jet Propulsion Laboratory

[45]. In the following, we describe a parallel effort at Goddard Space Flight Center using a low risk strategy using commercial foundry nodes with RHBD techniques [50][51][52][53][54] to fabricate a radiation hard MCD ASIC tolerant to 3 Mrad (Si) TID. Commercial foundry process nodes have the following advantages: (i) stable, non-iterating process node with a heritage of proven designs; (ii) a comprehensive and robust process design kit (PDK); (iii) regular tape-in schedules that are known well in advance; (iv) good support from the foundry, i.e. libraries, application notes, etc.; (v) ITAR compliant, preferably domestic source; (vi) available radiation data indicating some inherent radiation hardness and (vii) low cost. Both IBM [55] and TowerJazz [56] offer 180 nm CMOS nodes that are good candidate processes for the MCD ASIC. Both companies also offer an SOI variant. The use of SOI prevents Single Event Latch-up (SEL) in CMOS circuits. If RHBD techniques, such as enclosed layout transistors (ELT), are utilized in a process node which already has some TID tolerance (to at least 100 krad

(Si)) and SEL immunity (through SOI or RHBD) then a high TID/latchup immune ASIC can be built. A strategy to get to 3 Mrad (Si) TID is to have a design which (1) exceeds the specifications before irradiation, (2) is built in an unmodified process node with some inherent hardness to TID and (3) which is hardened with RHBD and/or SOI. RHBD here includes ELTs, guard-rings and circuit mitigation.

11.6.5 Choice of Technology

The choice of technology for manufacturing the MCD ASIC for thermopile array readout will be determined by the following requirements a) radiation hardness; b) speed, bandwidth, and die area; and c) cost. To this end, commercial processes offered by IBM and TowerJazz provide optimal tradeoffs. For example the 180 nm CMOS IBM technology is accessible with the following four processes a) 7SF, b)

7RF/7TG, c) 7HV, and d) 7RF SOI which are tailored for a) high performance graphics, communication and data processing, b) RF and wireless applications such as Bluetooth and LANs, c) power management products and display drivers, and d) RF switch applications to integrate multiple analog functions into single chip solutions, respectively [57]. Additionally variants such as 7HP and 7WL with cut-off frequencies approaching 130 GHz [55] offer BiCMOS solutions for wireless and high-speed applications. Furthermore the 130 nm IBM technology is accessible via CMOS-only processes 8RF and 8SFG, as well as BiCMOS processes 8HP and 8WL. Feature sizes as small as 90 nm, 65 nm, 45 nm and 32 nm are also available at IBM through the Trusted Access Program Office (TAPO) which has been chartered by the US Government to find and maintain suppliers of trusted microelectronic parts [58]. Moreover, TowerJazz Semiconductor provides 180 nm technology in CMOS-only, SiGE BiCMOS and CMOS thick-film SOI (with a 1000 Ω-cm high resistivity thick film SOI [56]) processes such as CA18, SBC18, and

CA18HB, respectively [59].

Among these processes, the SOI variants naturally possess single-event latchup immunity [60], but can suffer single-event snapback in the absence of well-designed body ties [61]. Silicon dioxide insulator layers enclosing the MOSFET channels increase possible exposure to TID effects [62][63]. Furthermore, for smaller feature sizes, a single heavy ion charge track may give rise to charge accumulation under the buried oxide and in the channels of multiple MOSFETs, resulting in upsets at multiple circuit nodes [64]. However, bulk CMOS processes are also prone to this type of multiple bit upsets in addition to being susceptible to single-event latchup (SEL). Besides the inherent weaknesses and strengths of bulk CMOS or SOI CMOS technologies, one should also take into consideration available devices and passives for each process. For example, even though the 7RF SOI process allows layout of most passives such as metal-insulator-metal capacitors and series/parallel spiral inductors, it only allows the layout of regular threshold voltage transistors [55]. For

niche applications, the designers might need high voltage or ultra-thin regular threshold voltage MOSFETs such as those in 7HV, or zero threshold or triple well field effect transistors included in 7RF [55]. A circuit designer might also prefer to choose CMOS processes with bipolar transistor options, which are not available in 7RF SOI, to design, for instance, voltage reference circuits.

11.6.6 Extreme Environment Integrated Circuit Modeling

The design and simulation of a complicated integrated circuit such as the MCD ASIC are challenging even for room temperature radiation-free operation from a circuit point of view. Any extreme circuit ambient such as high radiation and low temperature only makes the first-pass design and circuit optimization harder due to absence of harsh environment com-

pact models needed for circuit simulations. A specially developed extreme environment Computer Aided Design (CAD) tool or extreme environment physics based analytical device models are needed to obtain ASIC performance. This requires development of a CAD tool similar to the widely used Simulation Program with Integrated Circuit Emphasis (SPICE) [65][66] calibrated for operation at low temperatures and under high levels of radiation. Furthermore, this CAD tool needs to run in conjunction with the existing framework of integrated circuit design, and function along with foundry-supplied PDKs as well as tool sets including physical design (layout), Design Rule Check (DRC), and Layout-Versus-Schematic (LVS) software.

Comparatively speaking, there has been minimal effort to design electronics that operate reliably at low temperatures and under radiation which are typical conditions of those encountered in deep space missions, especially by Readout Integrated Circuits (ROICs) of sensors and detectors. For instance, mercury cadmium telluride infrared sensors [67]

along with their ROICs are usually exposed to relatively high levels of radiation and near 77 K temperatures. The current practices of IC design with PDK libraries and models generally involve use of room temperature models to design low temperature circuits, since setting the temperature lower than the calibrated range of models during circuit design generally leads to unpredictable actual performance at low temperatures [68]. Likewise, the radiation hard designs are based on the knowledge of empirical process statistics and known RHBD circuits such as enclosed MOSFETs and DICE [69] flip-flops. The additional nonlinearities observed in current-voltage curves measured at extremely low temperatures and high radiation give rise to challenges in the design of reliable and predictable circuits and systems. Typically, CMOS processes are designed for 300 K operation, and high radiation levels or low temperatures introduce uncertainty into the performance and long-term reliability of electronics because design tools and methodologies are built for room temperature and not for cryogenic temperatures in the range of 230 K or

less [70]. Commercial, industrial and military electronics design software packages are typically calibrated for temperature ranges of 273 K - 343 K, 233 K - 358 K, and 218 K - 398K, respectively. The details of the semiconductor physics that occur at cryogenic temperatures (< 230 K) and under radiation simply have not played a sufficiently large role in electronics design development to provide the existing knowledge base and CAD tool development necessary for robust cryogenic development.

In the past, operation at low temperatures was thought impossible due to carrier freeze-out. However modern MOSFET source-drain junctions are metallic due to their high doping levels. This places the Fermi level in the impurity band formed by the dopant atoms – there is no freeze-out in these regions. The mobile densities thus created allow rapid equilibration and population of the active channel with mobile charge. Also, at low temperatures, carrier mobility rises and junction capacitances decrease (due to larger space-

charge depths). All of these factors opt for improved performance at low temperature [68][71].

This does not mean that one can simply use existing computer-aided design tools to create complex integrated circuits operating at these temperatures. There is added physics that must be incorporated into the base models. These primarily pertain to impact-ionization models [68]. However the basic design formats of existing component parameter extraction schemes (such as BSIM [70][72] – a field-effect transistor compact model- of ICCAP [73] – integrated circuit characterization and analysis program) can be maintained [68][71]. Therefore modifications to standard SPICE models can be incorporated through re-scripting of the standard compact models (i.e., the formula set) used to create "theoretical" current-voltage (I-V) and time-dependent I-V response plots. These scripts shall also be immediately transportable to SPICE codes for high-level system modeling with existing commercial SPICE and design tools.

SPICE models are imperative for circuit design. However, BSIM models [70], which are the standard compact models used for MOSFET based circuit design, do not exist for high radiation levels or cryogenic temperatures. This limitation can be overcome using the circuit/analog behavioral programming language Verilog-A [74][75]. For example, Figure 11.6.3 shows 50 K and 150 K measurements and simulations for a 0.48 μm x 0.12 μm MOSFET. Here the fits are obtained via inclusion of low temperature physics into the standard BSIM model using a Verilog-A library specifically developed for IBM 8RF MOSFETs. The use of Verilog-A enables one to include low temperature and radiation models, and relevant new physics into standard BSIM models. It allows for circuit element model revision and creation that is extremely flexible and integrates smoothly into most circuit design SPICE-like computation engines. It is therefore one of the preferred modeling languages for implementing new and revised radiation and low temperature device models.

The addition of radiation effects into BSIM-type compact

models requires first the identification of important radiation effects for a given process, and then its incorporation into the model using physics-based analytical expressions. For instance, small feature size processes exhibit moderate threshold voltage shifts caused by gamma irradiation due to the small thickness of sensitive gate oxide present. This is incorporated into simulations by the introduction of new total dose parameters, and an attendant equation that reflects change in threshold voltage [76][77]. Additionally, the small feature size bulk MOSFETs are generally fabricated using shallow trench isolation (STI). This trench oxide plug charges positively [22] under irradiation, possibly inverting the sidewall of the trench and MOSFET channel and resulting in high leakage due to parasitic channel formation [78]. Such dose-dependent leakage levels incorporated into Verilog-A MOSFET models, for instance, by taking the Gate Induced Drain Leakage (GIDL) parameters in BSIM as a function of total dose, calibrated by experiments.

In summation, circuit designers require SPICE-type CAD

tools to design and simulate extreme environment circuitry. Since compact models such as BSIM3 and BSIM4 are not developed for operation under such extreme conditions, they lack relevant physics and corresponding analytical models. However, the analog behavioral languages such as Verilog-A can be used to modify the standard BSIM models, which can run in conjunction with the standard models in commercial SPICE simulators and process design kits.

11.6.7 MCD ASIC Design

The main function of the MCD, illustrated in Figure 11.6.5, is to amplify, integrate and digitize the outputs of a thermopile array. A summary of the specifications of the ASIC is given in Table 11.6.1. The amplification task is particularly challenging with respect to offset and noise as the pixel voltages generated by the thermopile range from hun-

dreds of nanovolts to only one or two hundred microvolts. A representative plot of output voltage versus scene temperature for a thermopile is shown in Figure 11.6.7. These slowly changing voltages must be greatly amplified (by as much as several thousand) and integrated before digitization, which places stringent demands on the noise and offset performance of the analog front end (AFE). Each of the 16 channels is comprised of a high impedance ground sensing buffer, auto-zeroed chopper amplifiers (to minimize 1/f noise) and an integrator. The 16 channels are multiplexed into one final amplifier that drives a 16-bit ADC with fully balanced differential signals. The gain in each channel is variable and controlled by a user supplied 4-bit word. The gains have a roughly exponential relationship to the gain code (illustrated in Figure 11.6.6). A variable gain allows the user to optimize the SNR depending on the thermopile signal amplitudes. An integrator following each demodulator (prior to the multiplexer) performs an averaging function on the amplified signals, which removes most of the chopper tones

and high frequency noise.

Each channel outputs an amplified and filtered signal, which is fed to a final buffer amplifier through a 32:1 multiplexer. One of the channels is dedicated to the temperature sensor while the remaining 15 are used for monitoring critical nodes for self-test purposes. During a normal data collection run, the multiplexer is switching from channel to channel with a cycle time of 17 channel sampling intervals. The channel sampling interval is determined by the required frame rate, where a frame represents the digitized data for all 17 signals (pixels plus temperature sensor). The frame rate can be as high as 20 frames per second (fps). Thus all of the data associated with each of the 17 channels must be unloaded in 50ms which is equivalent to 1 channel approximately every 3ms. Thus the effective ADC conversion rate is 340 samples per second.

The ADC is an algorithmic (cyclic) architecture generating 3 bits per clock cycle and 16-bits every 8 clock cycles. A clock cycle lasts 200 ns so a full 16-bit conversion requires

1.6us, equivalent to a sample rate of 625 kHz. Since the AFE ADC sample rate only needs to be a few hundred Hertz, oversampling is used to improve the signal-to-noise ratio (SNR) and realize additional bits through averaging. Each octave of oversampling beyond the Nyquist rate (2X bandwidth) yields an additional half bit (3dB) of SNR improvement. In the MCD, an extra 5 bits from oversampling is realized pushing the effective number of bits (ENOB) to 21.

In order to minimize the effects of 1/f noise and offsets, each channel modulates its input before amplification. The amplified signals are then demodulated and integrated for quantization by the ADC. The signal processing sequence is as follows:

1. Frequency translate (modulate) the input signal to harmonics of the chopper (clock) rate;
2. Amplify with auto-zero;
3. Demodulate the amplified signal:
    a. Amplified signal goes back to baseband

b. Offsets & 1/f noise shifted up to harmonics of the chopper frequency;

4. Filter and apply more variable gain;
5. Integrate the result;
6. Multiplex and buffer;
7. Digitize at integral sub-multiple of chop rate where any stray chop tones alias down to DC.

The chopping is performed with “passive circuits” using switches to perform the modulation/demodulation. The chopping occurs at a rate of 64kHz to 128kHz. The single-ended input signal referenced to the imager’s ground potential is modulated and amplified by a two-stage amplifier yielding a gain of several thousand. The amplified signal is then demodulated and integrated. The integrator output is multiplexed into a buffer amplifier that drives the ADC.

The output of the demodulator is filtered and integrated but may still have chop tones indirectly coupled through substrate parasitics and the supplies. Sub-sampling this with the

ADC removes the chop tones. In practice, the amplifier must also be auto-zeroed since the offsets can be higher than 1mV and the high gain could saturate the output stages. The gain is implemented in three stages: the first two gains occur before demodulation, with the third after the demodulator.

11.6.8 MCD ASIC RHBD Techniques

RHBD is employed to compensate for cumulative and spontaneous radiation effects. Cumulative radiation effects caused by TID tend to increase the threshold voltages of PMOS transistors and decrease them in NMOS transistors, although this effect scales with the process node (thinner oxides provide less volume in which to capture and store the TID induced positive charge [79][80]). More damaging are the effects TID has on leakage and displacement damage dose (DDD), which degrades mobility [81] of non-hardened

NMOS devices. Accumulated positive charges in the thicker field oxide boundaries around each NMOS transistor can cause parasitic conduction paths from drain-source (through virtual NMOS devices in parallel with their hosts) and between adjacent NMOS devices with different drain/source potentials. This raises the off-state power dissipation, lowers the gain of the transistor through increased drain-source conductance, decreases the isolation between affected nodes and renders switches always on to some extent. Eventually, TID can cause total failure of a circuit.

TID's impact on the NMOS transistors is the main focus of hardening for cumulative radiation effects. The classic strategy to mitigate these effects is to harden the NMOS in the physical design using n+/p+ diffusion guard rings and edgeless transistors (ELTs). These techniques, though effective, incur area, power and performance (e.g. parasitic capacitance) penalties.

Spontaneous events are termed single event effects (SEEs) which include SEL, single event transients (SETs) and single

event upsets (SEUs). Latchup after a single event strike is particularly hazardous, as the result can be an open circuit in the metal conductors caused by electron migration due to high-induced currents. At best, SEL may just render the circuit inoperable until the power supply is switched off and back on again. SETs and SEUs affect both the analog and digital portions of an ASIC by causing voltage/current/bit changes, which perturb a signal from its correct value. Such perturbations in the analog circuit could manifest as errors picked up in the quantization or maybe temporarily destabilize an otherwise stable amplifier loop. In digital circuits, bit patterns can get corrupted which might, in the worse case, cause high current situations, which ultimately shorten the life of the chip. SET, SEUs and SEE errors in general, though, can either be flushed out, scrubbed (if detected) or protected against using temporal latches or triple mode redundancy.

The process node chosen for the MCD is TowerJazz's CA18 which has been extensively evaluated for radiation hardness,

both within NASA and externally. The thin gate oxide of the 180nm FETs provides inherent resistance to threshold voltage shifts caused by TID [52][82]. The CA18 process uses STI and coupled with the lower supply voltages this helps to reduce the general sensitivity to SEL [83]. However, the STI is a contributing element in the onset of TID induced leakage. The baseline hardness for this process node is at least 100 krad (Si) TID with no RHBD. The process also offers a thick oxide FET variant, which allows operation at 3.3 V (nominal), which is useful for large swing signals and input/output (I/O) circuits. Table 11.6.2 provides measured leakage data for four standard geometry 3V NFET devices with different widths (W) and lengths (L) before and after 300 krad (Si) TID radiation. The measurements were performed at room temperature (T_A~300 K) with Vds=3.3 V, Vgs=0 V and Vbs=0 V. The column reporting the ratio of post to pre-rad measurements indicates that the device with the 10 μm width and 10 μm length faired best from this relatively low TID exposure. This tracks the trend seen in the

thin oxide devices, data for which is illustrated in Figures 11.6.8-11.6.10. In some areas of the MCD (e.g. certain cascode devices), long and/or wide standard geometry NMOS biased in the fully saturated region were used.

The MCD ASIC takes a multi-path approach to RHBD, employing both circuit and layout enhancements to raise the tolerance to TID and single events. In the amplifier, comparator and bias current generator circuits, standard low voltage design techniques are employed with adaptive bias to compensate for threshold voltages that vary with temperature, age and radiation. Utilizing a front to back fully differential signal path also helps to harden the circuit against TID induced changes in the common mode (CM) levels of analog voltages. Thus all of the amplifier and ADC circuits use fully balanced differential signal paths, which also enhances linearity and noise rejection. Since the TID mechanism has a more severe effect on NMOS devices, PMOS is employed in the first instance wherever possible. For example, the input differential pair of the OTAs are PMOS, which facilitates the

incorporation of ELT NMOS as gm multiplier or folded cascode loads.

The ELT, while reportedly the best hardening mechanism for an NMOS, has several caveats requiring special attention. ELTs are inherently asymmetric with a large difference in the drain and source areas, have higher gate capacitances (than their standard geometry counterparts) and occupy a larger die area for equivalent W/L ratios. The layout of an 8 x 2 array of ELT NMOS transistors is illustrated in Figure 11.6.11. Reliability and low output conductance requirements point to using an outer drain region in the layout of the device [52][83]. The asymmetry also results in a difference between the drain- and source-to-bulk capacitances, which has implications for switched capacitor circuit designs [84]. Since SPICE models for ELTs are not currently (2011) included in most, if not all, foundries' process design kits (PDKs), the models are often approximations derived from standard geometry devices customized by the designer [52]. In the MCD analog sections, ELTs are not used for all

NMOS devices mainly because of the lack of an adequate model and the asymmetry. But ELTs are deployed universally in “bottom of the stack” areas such as NMOS current mirrors and load devices in PMOS differential pairs. TID induced drain-source leakages in the stacks with ELTs at the bottom are thus reduced to zero. For example, a common stack in the design is a cascoded current source comprised of two NMOS in series, illustrated in Figure 11.6.12. The standard geometry cascode device is always biased in a fully saturated mode where the effect of the TID induced parasitic device is minimized. But all NMOS (and PMOS) are guard ringed to prevent device-to-device leakage and SEL. Transmission gates (switches having both NMOS and PMOS devices in parallel) in the MCD’s analog multiplexer circuits and the ADC also utilize ELT NMOS.

RHBD in the digital areas of the design, such as the clock signal generators, registers, control logic and input/output circuits also utilizes guard rings and ELTs, along with circuit enhancements, which harden against SETs and SEUs. Dual

interlock cell (DICE) [83] latches are used in all registers to harden against SEUs. Since the system is a pipeline of analog and digital signals and no feedback loops involve digital quantities, most upsets experienced in the analog/digital sections will eventually get flushed out. There are two exceptions to this and these are in the registers containing the multiplexer channel number and channel gain settings. An upset experienced in these areas could throw off the channel number and gain, resulting in incorrect output data. To mitigate this, these registers are interfaced through a hardened serial port back to the application, which periodically reads their values to check that they are correct. The use of a read back verification in the ASIC is a key component of the digital RHBD techniques employed as it informs the application of the status of critical areas in the ASIC. Read back verification always occurs when a control word is up-dated in the MCD by the application.

The techniques used to harden the ASIC are summarized in the table below. In the table, “Cct” and “Lay” refer to circuit

and layout implementations; “A” and “D” refer to analog and digital; “RHBD Target” is the effect targeted by the hardening scheme.

11.6.9 Summary

Future missions to Jupiter and its satellites will require the robust design and manufacture of low mass electronics that consume low power and that operate with optimal performance in its cold and extremely harsh radiation environment. A strategy for meeting mission requirements is to fabricate ASICs with excessive operating requirement margins together with prudent radiation shielding to mitigate against gradual performance degradation from cumulative ionization and displacement damage effects.

Designing integrated circuits for this extreme environment will require careful determination of processes to be used for

ASIC designs. The choice is based on the inherent radiation hardness and temperature dependency of a process, as well as the availability of harsh environment design models, and component base for laying out radhard structures. Specifically, the technology node shall have at least 100 krad (Si) radiation immunity and to provide design base for RHBD circuits. Secondly, the component base and available libraries are provided by the fabrication clearing house or foundries, and the lack of some components such as high voltage MOSFETs may render higher susceptibility to threshold voltage fluctuations due to TID induced oxide charging or low temperatures. Lastly, design tools and methodologies should exist for low temperature and under radiation operation. This requires development of extreme environment models that function along foundry-supplied process design kits as well as commercial IC design tools. To this end, the analog behavioral programming language Verilog-A is used to modify the standard BSIM compact model set to include low temperature and radiation induced threshold voltage shifts, rises in

subthrehold leakage, effects on mobility etc. Here Verilog-A allows for circuit element model revision and creation that is extremely flexible and integrates smoothly into commercial SPICE-like computation engines. Also, low temperatures and radiation give rise to subtle changes in device operation, generally enabling use of standard MOSFET compact model sets such as BSIM with addition of new physics related to low temperature and radiation.

The Multi-Channel Digitizer (MCD) ASIC was designed to interface directly to a thermopile array for remote sensing of Europa's surface temperature. The MCD has 16 low noise, low offset image pixel gain channels and one array temperature sensor channel which interface to an onboard 16-bit analog to digital converter (ADC). Each channel contains a modulator, auto zeroed gain stages, a demodulator and an integrator. The channels are selected one by one through a 32:1 multiplexer to be digitized by the ADC. The MCD incorporates RHBD techniques to allow the ASIC to operate up through 3 Mrad (Si) TID in the Jovian system. RHBD also

includes hardening to single event effects, such as latchup (SEL), single event transients (SETs) and single event upsets (SEUs). The ASCI is fabricated in a 180 nm commercial bulk CMOS process node used extensively for industrial, military and commercial ASIC development.

References

[1] T. V. Johnson, C. M. Yeates, and R. Young, "Volume on Galileo Mission Overview," *Space Science Reviews*, vol. 60, pp. 3-21, 1992.

[2] D. M. Harland, *Jupiter Odessey: the story of NASA's Galileo Mission*.: Praxis Publishing, Springer-Verlag, 2000.

[3] R. O. Fimmel, W. Swindell, and E. Burgess, "Pioneer Odyssey, Encounter with a Giant," NASA, Washington DC, SP-349 1974.

[4] R. O. Fimmel, J. Van Allen, and E. Burgess, "Pioneer, First to Jupiter, Saturn and Beyond," NASA, Washington DC, SP-446 1980.

[5] D. Morrison and J. Samz, "Voyage to Jupiter," NASA, Washington DC, SP-439 1980.

[6] D. Morrison, "Voyage to Saturn," NASA, Washington DC, SP-451 1982.

[7] D. Morrison, Ed., *The Satellites of Jupiter*. Tucson, Arizona, USA: The University of Arizona Press, 1982.

[8] M. J. S. Belton, "Special Issue of Remote Sensing Results of the Galileo Orbiter Mission," *Icarus*, vol. 135, pp. 1-376, 1998.

[9] D. Fischer, *Mission Jupiter: The Spectacular Journer of the Galileo Spacecraft*. New York, NY, USA: Spinger-Verlag, 2001.

[10] C. Zimmer, L. Kurana, and M. G. Kivelson, "Subsurface Oceans on Europa and Callisto: Constraints from Galileo Magnetometer Observations," *Icarus*, vol. 147, pp. 329-347, 2000.

[11] R. T. Pappalardo, W. B. McKinnon, and K. Khurana,

Europa. Tucson, AZ, USA: The University of Arizona Press, 2009.

[12] National Research Council - Space Studies Board, "A science startegy for the exploration of Europa," Washington DC , 0309064937, 1999.

[13] M. T. Bland, A. P. Showman, and G. Tobie, "The orbital-thermal evolution and global expansion of Ganymede," *Icarus*, vol. 200, pp. 207-221, 2009.

[14] F. Bagenal, T. E Dowling, and W. B. McKinnon, *Jupiter: The Planet, Satellites and Magnetosphere*. New York, NY, USA: Cambridge University Press, 2007.

[15] K. Clark et al., "Return to Europa: Overview of the Jupiter Europa orbiter mission," *Advances in Space Research*, vol. 48, pp. 629-650, 2011.

[16] K. Clark et al., "Europa Jupiter System Mission," Prepared by: Joint Jupiter Defintion Team NASA/ESA Study Team, A Joint Endeavour by ESA and NASA, 2009.

[17] The NASA Element of the Europa Jupiter Mission (EJSM), "Jupiter Europa Orbiter Mission Study 2008. Final Report," NASA, Washington DC, NMO710851 2008.

[18] ESA contribution to the Europa Jupiter System Mission, "Jupiter Ganymede Orbiter," ESA-SRE(2008)2 2009.

[19] "Vision and Voyages for Planetary Science Decade 2013-2022," NRC of the National Academies, 100309209544, 2011.

[20] J. Van Cleve, Pappalardo R., and J. Spencer, "Thermal palimpsests on Europa: how to detect sites of current activity," in *30th Annual Lunar and Planetary Science Conference, March 15-29th*, 1999.

[21] O. Abramov and J. Spencer, "Numerical modeling of endogenic thermal anomalies on Europa," *Icarus*, vol. 195, no. 1, pp. 378-385, 2008.

[22] R. H. Maurer, M. E. Fraeman, M. N. Martin, and D. R. Roth, "Harsh Environments: Space Radiation Environments, Effects, and Mitigation," *Johns Hopkins APL Technical Digest*, vol. 28, no. 1, pp. 17-29, 2008.

[23] A. J. Dessler, *Physics of the Jovian Magnetosphere*. New York, NY: Cambridge University Press, 2002.

[24] J. Connerney, M. Acuna, N. Ness, and T. Satoh, "New models of Jupiter's magnetic field constarined by the Io flux tube footprint," *J. Gepphys. Res.*, vol. 103, no. A6, pp. 11929-11939, 1998.

[25] K. K. Khurana and N. A. Tsyganeko, "Towards a global magnetic field of Jupiter's magnetospher derived from observations of Galileo and previous missions," in *AGU meeting, 17-21 May 2004 , Montreal, Canada*, 2004.

[26] J. S. Lewis, *Physics and Chemistry of the solar system*.: Elsevier Acadamic Press, 2004.

[27] W. Fillius, *The Trapped Radiation Belts of Jupiter: Studies of the interior, atmosphere, magnetosphere, and satellites*, Gehrels T., Ed. Tucson, AZ, USA: The University of Arizona Press.

[28] C. F Kennel and F. V. Corotini, "Jupiter's Magnetosphere," *Ann. Rev. Astron. Astrpphys.*, vol. 15, pp. 389-436, 1977.

[29] K. K. Khurana et al., "The configuration of Jupiter's magnetosphere," in *Jupiter: The Planet, Satellites and Magnetosphere*, T. E. Dowling, W. B. McKinnon F. Bagenal, Ed. New York, NY, USA: Cambridge University Press, 2004.

[30] P. D. Fiesler, S. M. Ardalan, and A. R. Frierickson, "The radiation effects on Galileo Spacecraft Systems at Jupiter," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, 2002.

[31] H. B. Garrett, "JEO Spacecraft Environments," in *EJSM 4th Instrument Workshop*, LA, Universal City, CA, 2010, http://opfm.jpl.nasa.gov.

[32] T. N. Divine and H. B. Garrett, "Charged particle distributions in Jupiter's magnetosphere," *J. Geophys. Res.*, vol. 88, pp. 6889-6903, 1983.

[33] H. B. Garrett et al., "Galileo Interim Radiation Electron Model," The Jet Propulsion Laboratory, California Institute of Technology, Pasadena, 03-006 2003.

[34] H. Garrett, M. Kokorowski, I Jun, and R. Evans, "Galileo Interim Radiation Electron Model Update - 2011," in *EPCS Abstracts, EPSC-DPS Joint Meeting, EPSC-DPS2011-1731*, vol. 6, 2011.

[35] D. J. Williams, R. W. McEntire, S. Jaskulek, and B. Wilken, "The Galileo energetic particle detector," *Space Sci. Rev.*, vol. 60, pp. 385-412, 1992.

[36] T. L. Garrard, N. Gehrels, and E. C. Stone, "The Galileo heavy element monitor," *Space Sci. Rev.*, vol. 60, pp. 305-315, 1992.

[37] C. Paranicas et al., "Europa's near-surface radiation environment," *Geophys. Res. Lett.*, vol. 34, no. L15103, 2007.

[38] T. Jordan, "NOVICE: A radiation transport/shielding code users guide," Experimental and Mathematical Physics Consultants, 2000.

[39] T. Jordan, "The accuracy of NOVICE electron shielding calculations," in *Proc. 1st Eur. Conf. on radiation and its effects on Devices and Systems RADECS 91, Sep. 9-12*, 1991, pp. 320-324.

[40] I. Jun, H. B. Garrett, and Evans. R., "High Energy Trapped Particle Environments at Jupiter: An update," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, 2005.

[41] R. A. Hanel, B. J. Conrath, D. E. Jennings, and R. E. Samuelson, *Exploration of the Solar System by Infrared Remote Sensing*, 2nd ed. New York, New York, United Staes of America: Cambridge University Press, 2003.

[42] D. A. Paige et al., "The Lunar Reconnaissance Orbiter

Diviner Lunar Radiometer Experiment," *Space Sci. Rev.*, vol. 150, pp. 125-160, 2010.

[43] U. Dillner et al., "A 64-pixel linear thermopile array chip designed for vacuum environments," in *Proceedings of IRS 2006, Nunberg, 30-31 May 2006, Sensor + Test 2006 Proceedings*, Nunberg, 2006, pp. 295-300.

[44] M. C. Foote et al., "Thermopile Detector Arrays for Space Science Applications," in *Proceedings of the TDW'03 International Thermal Detectors Workshop*, Washington DC, 2003.

[45] S. Gaalema, S. Van Duyne, J. L. Gates, and M. C. Foote, "Thermopile detector radiation hard readout," in *Proc. of SPIE, Detectors and Imaging Devices: Infrared, Focal Plane, Single Photon*, vol. 7780, 2010.

[46] J. P. Fleurial, "Design and Discovery of Highly Efficient Thermoelectric Materials," in *International Union of Materials Research Society*, Florence, Italy, 1998, pp. 1-13.

[47] M. Citterio, S. Rescia, and V. Radeka, "Radiation effects at cryogenic temperatures in Si-JFET, GaAs MESFET, and MOSFET devices," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 2266-2270, Aug. 2002.

[48] I. Jun, "Shielding Design," in *EJSM 4th Instrument Workshop, July 26-29*, LA, Universal City, CA, 2010, http://opfm.jpl.nasa.gov.

[49] S. Aslam, "Europa Radiometry," Planetary Systems Laboratory, NASA GSFC, Greenbelt, MD, Internal Document 2011.

[50] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2413-2420, 2005.

[51] R. N. Nowlin, S. R. McEndree, A. L. Wilson, and D. R. Alexander, "A new total-dose induced parasitic effect in

enclosed-geometry transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2495-2502, 2005.

[52] L. Chen and D. M. Gingrich, "Study of N-Channel MOSFETs With an Enclosed-Gate Layout in a 0.18 um CMOS Technology," *IEEE Transactions on Nuclear Science*, vol. 52, no. 4, pp. 861-867, August 2005.

[53] R. C. Locoe, J. V. Osborn, R. Koga, S. Brown, and D. C. Mayer, "Application of hardness-by-design methodology to radiation-tolerant ASIC technologies," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, 2000.

[54] J. E. Hubbs, M. E. Gramer, D. Maestas-Jepson, G. A. Dole, and A. Hahn, "The impact of Radiation Hardened By Design (RHBD) Techniques on the Performance of Readout Integrated Circuits in Radiation Environments," in *Proc. of SPIE*, vol. 7095, 2008.

[55] (2011, September) MOSIS IBM processes. [Online]. http://www-03.ibm.com/technology/foundry/index.html

[56] (2011, September) Tower/Jazz Semiconductor. [Online]. http://www.towerjazz.com/pdf/CMOS_SOI.pdf

[57] (2011, September) MOSIS Web site. [Online]. http://mosis.com/ibm/ibm_processes.html

[58] (2011, September) TAPO Office. [Online]. https://www.tapoffice.org/

[59] (2011, September) Tower/Jazz SOI. [Online]. http://www.jazzsemi.com/technology.html

[60] J. P. Colinge, *Silicon on Insulator: Materials to VLSI*. New York: Kluwer, 1991.

[61] P. E. Dodd et al., "Single-Event Upset and Snapback in Silicon-on-Insulator Devices and Integrated Circuits," *IEEE Trans. on Nuclear Science*, vol. 47, pp. 2165-2174, December 2000.

[62] V. Ferlet-Cavrois et al., "Worst-Case Bias During Total

Dose Irradiation of SOI Transistors," *IEEE Trans. on Nuclear Science*, vol. 47, pp. 2183-2188, December 2000.

[63] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation Effects in SOI Technologies," *IEEE Trans. on Nuclear Science*, vol. 50, pp. 522-538, June 2003.

[64] D. F. Heidel et al., "Single-Event Upsets and Multiple-Bit Upsets on a 45 nm SOI SRAM," *IEEE Trans. on Nuclear Science*, vol. 56, no. 6, pp. 3499 - 3504, December 2009.

[65] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with Spice*, 2nd ed. United States of America: McGraw-Hill, 1993.

[66] (2011, September) The Spice Home Page. [Online]. http://bwrc.eecs.berkeley.edu/classes/icbook/spice/

[67] L. H. Kidder, I. W. Levin, E. N. Lewis, V. D. Kleiman, and E. J. Heilweil, "Mercury cadmium telluride focal-plane array detection for mid-infrared Fourier-transform spectroscopic imaging," *Optics Lett.* , vol. 22, no. 10, pp. 742-744, May 1997.

[68] A. Akturk et al., "Compact modeling of 0.35mm SOI CMOS technology node for 4K dc operation using Verilog-A," *Microelectronic Engineering*, vol. 87, no. 12, pp. 2518-2524, 2010.

[69] T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *IEEE Trans. on Nuclear Science*, vol. 43, no. 6, pp. 2874-2878, December 1996.

[70] (2011, September) BSIM Homepage. [Online]. http://www-device.eecs.berkeley.edu/bsim3/

[71] A. Akturk et al., "Compact and distributed modeling of cryogenic bulk mosfet operation," *IEEE Transactions on Electron Devices*, vol. 57, no. 6, pp. 1334-1342,

2010.

[72] (2011, September) The Compact Model Council. [Online]. http://www.eigroup.org/cmc/

[73] (2011, September) Integrated circuit characterization and analysis program: ICCAP. [Online]. http://www.agilent.com/find/eesof-iccap

[74] K. S. Kundert and O. Zinke, *The Designer's Guide to Verilog-A*.: Kluwer, 2004.

[75] G. J. Coram, "How to (and how not to) write a compact model," in *Behavior Modeling and Simulation Conf. (BMAS)*, 2004, pp. 97-106.

[76] J. R. Srour and J. M. McGarrity, "Radiation Effects on Microelectronics in Space," *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1443-1469, November 1988.

[77] T. R. Oldham, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. on Nuclear Science*, vol. 50, no. 3, pp. 483-499, June 2003.

[78] H. J. Barnaby, M. Mclain, and I. S. Esqueda, "Total-ionizing-dose effects on isolation oxides in modern CMOS technologies," *Nuclear Instruments and Methods in Physics Research B*, vol. 261, no. 1-2, pp. 1142-1145, August 2007.

[79] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation effects in MOS capacitors with very thin gate oxides at 80 K," *IEEE Trans. Nucl. Sci.*, vol. NS-31, pp. 1249-1255, Dec. 1984.

[80] Mario G. Ancona, and John A. Modolo Nelson S. Saks, "Generation of interface states by ionizing radiation in very thin MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-33, no. 6, pp. 1185-1190, Dec. 1986.

[81] V. Liberali, A Radiation Hardened-By-Design SRAM Memory in Commercial CMOS Technology, May 21, 2010.

[82] N. Dodds and J. Pellish, "Total Ionizing Dose Test Results for CA18HA FETs and Ring Oscillators," Flight Data Systems & Radiation Effects Branch, NASA GSFC, Internal Communication 2011.

[83] F. Faccio, "Design Hardening Methodologies for ASICs," in *Radiation Effects on Embedded Systems*.: Springer, 2007, pp. 143-160.

[84] M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo., E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, W. Snoeys G. Anelli, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," *IEEE Trans. on Nucl. Sci.*, vol. 46, no. 6, pp. 1690-1696, Dec. 1999.

[85] CoolCAD Electronics LLC. CoolCAD LLC Web site. [Online]. http://www.coolcadelectronics.com

TABLES

Table 11.6.1. MCD ASIC specifications

Parameter	Value
Supply voltage	1.80 V
Supply current	70 mA
Number of TP Channels	16
Number of TS channels	1
Signal to noise ratio	> 256
TP signal amplitude	0.1 – 120 μV
Gain (variable)	162 – 6.7k
Chopper frequency	64 - 128 kHz
Noise	10 nV/Hz
Ambient temperature	150 – 300 K
ADC Resolution	16 - 20 Bits
Integral Non-Linearity	4.0 LSB
Differential Non-Linearity	0.5 LSB
ADC Offset	1 % of Full-scale
Gain error	1 % of Full-scale
Channel – channel isolation	-40 dB
ADC Sample rate	340 Hz
OSR (variable)	1 - 16
Output Data Rate (OSR =1)	625 kHz

Table 11.6.2. Effect of 300 krad (Si) TID on 3V standard NMOS FETS of varying Ws / Ls

W	**L**	**I_1=Ids_{PRE}**	**I_2=Ids_{POST}**	**I_2/I_1**
µm	µm	A	A	
0.36	0.34	3.03E-10	1.10E-05	36303.63
10.00	0.36	3.68E-10	1.84E-06	5000.00
0.40	10.00	1.28E-10	3.00E-08	234.38
10.00	10.00	4.54E-10	4.91E-09	10.81

Table 11.6.3. RHBD techniques used in the MCD design

RHBD Technique	Cct	Lay	A	D	RHBD Target
PMOS implementation	√		√		TID
ELT NMOS		√	√	√	TID
Long / wide channel NMOS	√		√	√	TID
Adaptive bias	√		√		TID
Differential paths	√		√		TID
Guardrings		√	√	√	SEL
Low resistance well contacts		√	√	√	SEL
Non-minimum well spacing		√	√	√	SEL
DICE latches	√			√	SET/SEU
Read back verification	√			√	SET/SEU

FIGURES

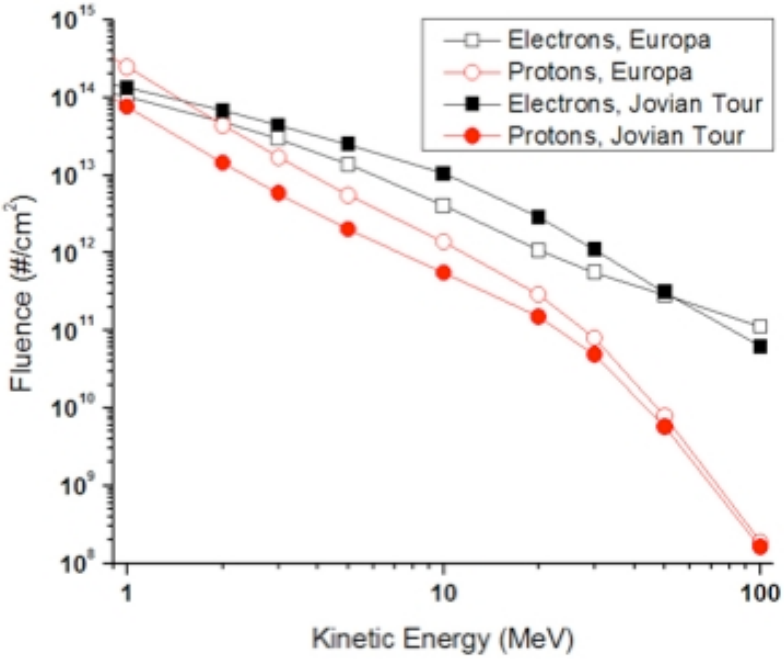

Figure 11.6.1. Electrons and protons fluence integral energy spectrum for JEO mission [17].

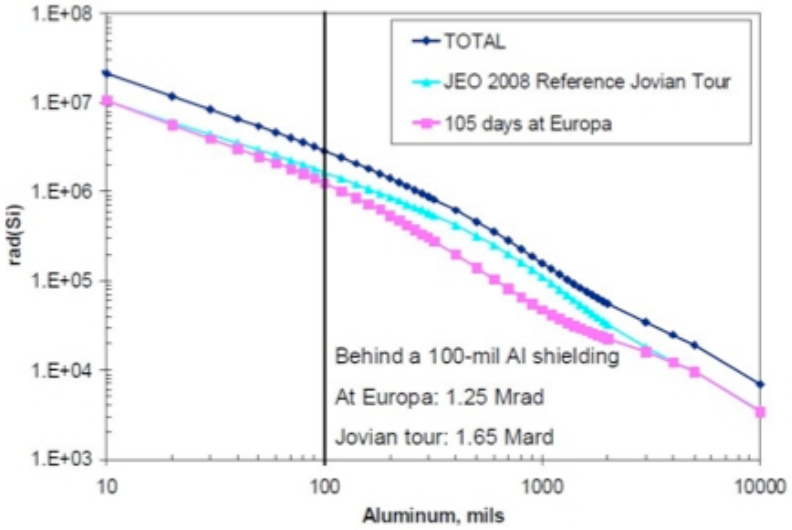

Figure 11.6.2. JEO Mission dose-depth curve for aluminum shielding [17].

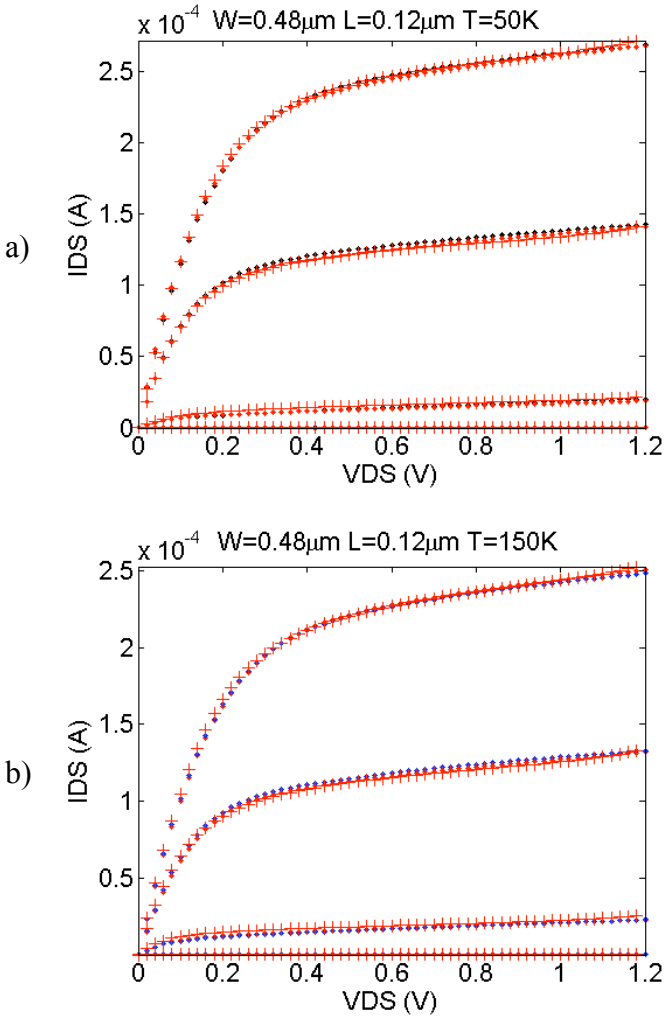

Figure 11.6.3. a) 50 K and b) 150 K measurements (dots) and SPICE simulations (pluses) for a 0.48 µm x 0.12 µm MOS-FET. Low temperature physics are incorporated into the standard BSIM model using a Verilog-A library specifically developed for IBM 8RF MOSFETs [85].

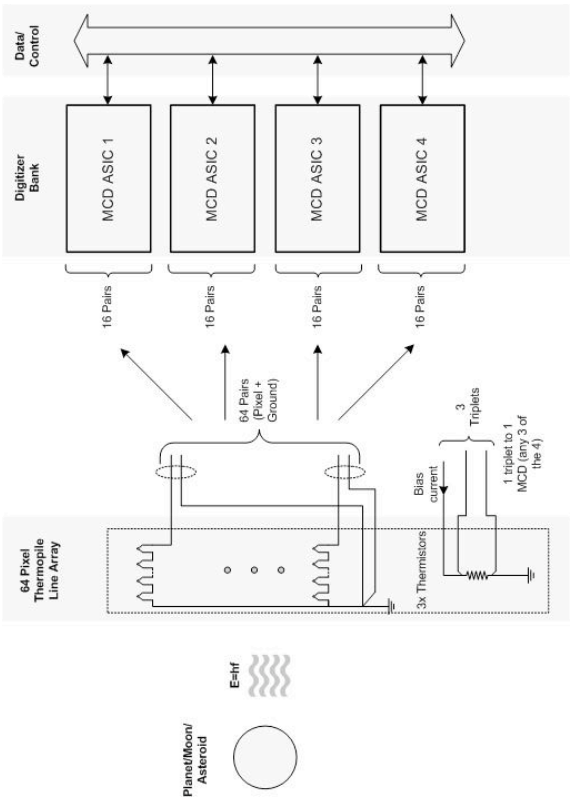

Figure 11.6.4. Thermopile - MCD application

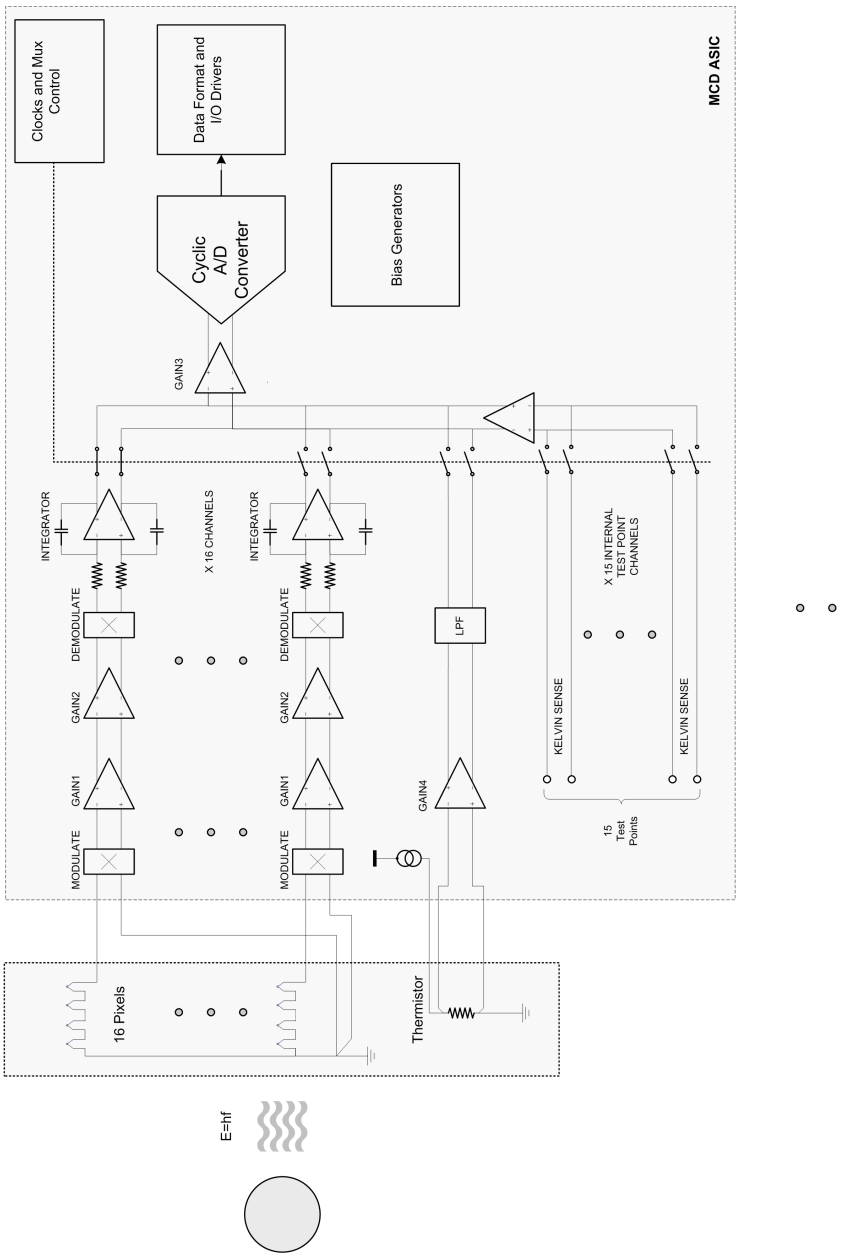

Figure 11.6.5. MCD top-level schematic

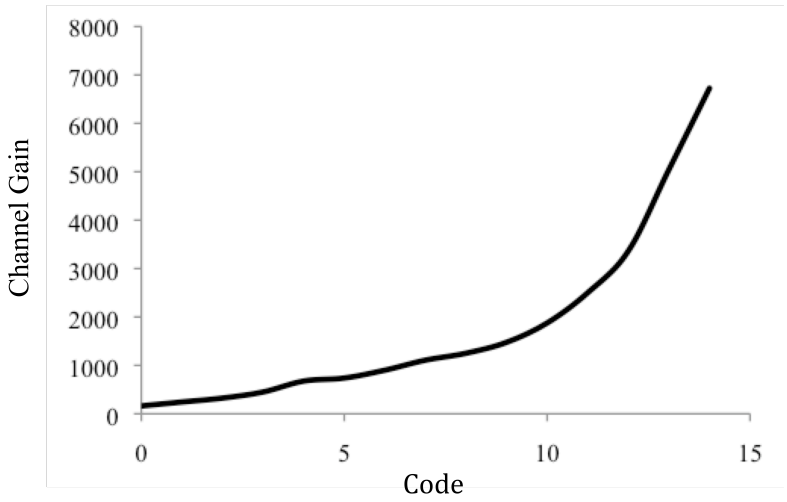

Figure 11.6.6. Channel gain vs. code

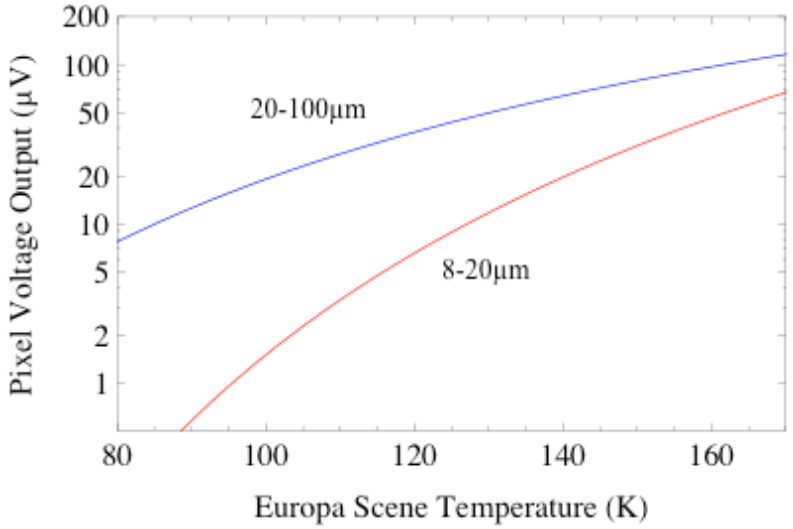

Figure 11.6.7 Pixel voltage output vs. Europa scene temperature **[49]**

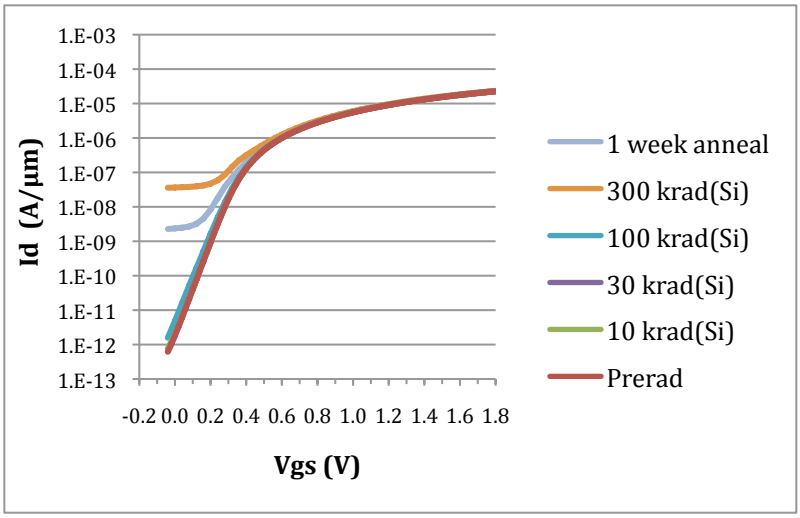

Figure 11.6.8. Ids (A/um) vs. Vgs (Vds=1.8V) for NMOS W=10µm L=10µm **[82]**

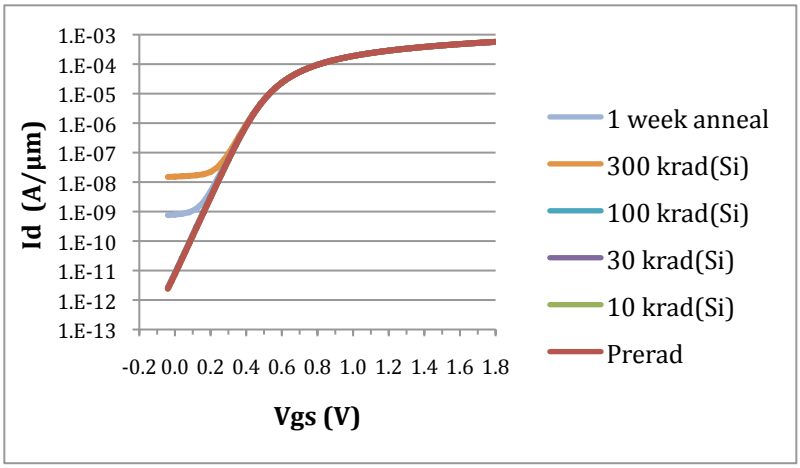

Figure 11.6.9. Ids (A/µm) vs. Vgs (Vds=1.8V) for NMOS W=10µm l=1.8µm **[82]**

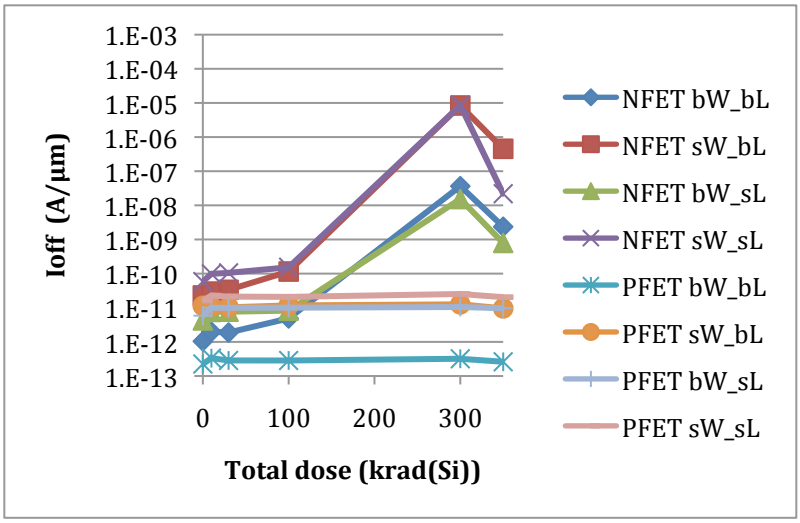

Figure 11.6.10. Off-state Ids (A/µm) vs. TID for 1.8V FETs
[82]

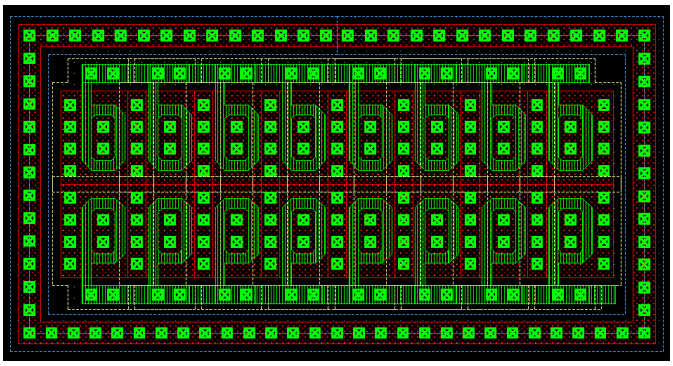

Figure 11.6.11. An 8 x 2 array of ELT NMOS devices

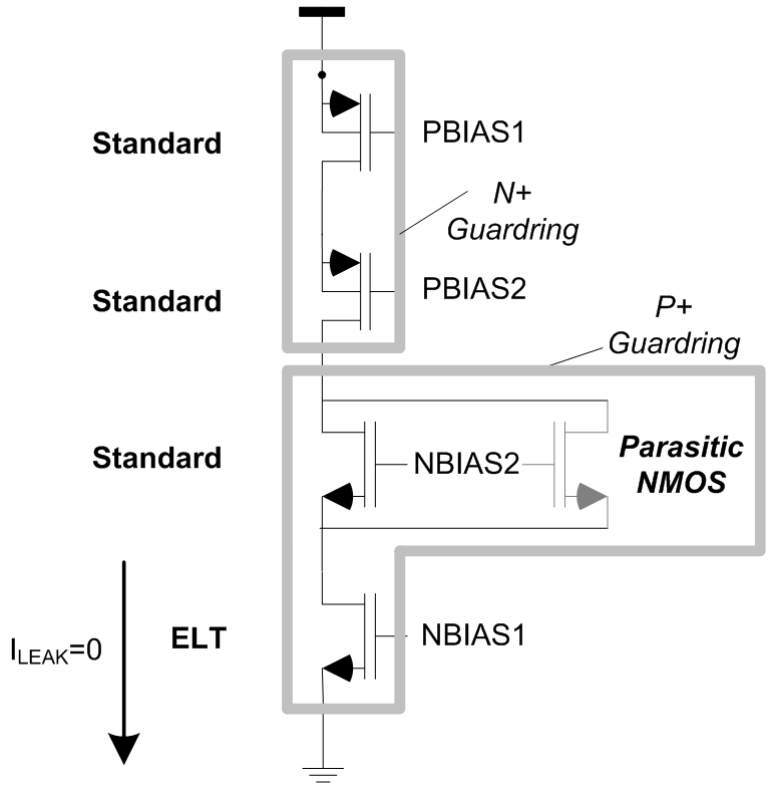

Figure 11.6.12. CMOS stack with ELT and standard geometry NMOS and guard rings