BACKPLANE DESIGN CONSIDERATIONS FOR HIGH SPEED SPACEWIRE NETWORKS

Session: Missions and Applications

Long Paper

Shahana Aziz Pagen

MEI Tech Inc., NASA Goddard Space Flight Center, Greenbelt, Maryland, USA

E-mail: Shahana.A.Pagen@nasa.gov

ABSTRACT

SpaceWire is becoming a preferred protocol for board to board communication over a backplane in addition to its existing use over cabled interfaces, replacing other protocols due to its simplicity and readily available flight quality physical layer devices, IP cores and test equipment. However, without specific guidelines for implementing SpaceWire over a backplane, designers are left to make trade decisions regarding connector selection, layout design rules and test accessibility issues. This paper will discuss NASA's Goddard Space Flight Center's implementation of high speed SpaceWire over backplane on James Webb Space Telescope and other missions.

1 INTRODUCTION

SpaceWire has been used for several years for communication between spacecraft sub-systems over a shielded twisted pair cable interface. The SpaceWire interface is well suited for long length cables, while maintaining the signal quality required for high speed propagation. The SpaceWire standard has well defined specifications for the necessary design considerations for communicating over cabled interfaces.

However, SpaceWire can also be used within a sub-system for communicating between cards connected by a printed circuit board (PCB) interface (such as a backplane). SpaceWire has several advantages over other backplane based communication protocols like CompactPCI; with its relatively simple software interface, fault tolerance support, high data throughput and ease of expansion using nodes and routers. However, unlike CompactPCI, which has a well defined backplane standard; there are no rules or recommendations established in the SpaceWire standard that addresses the unique challenges of designing this interface for a backplane. While several cable based design considerations still apply, there are other design considerations that are unique to this application but not addressed in the SpaceWire standard. This can leave designers unsure of how to implement the protocol to achieve desired performance as well as meet adequate design margins.

Test and verification access is another area where currently available test equipment and test methodologies may not be adequate when the interface operates across a backplane. While most available test equipment has built in interfaces to the SpaceWire defined connector; it is up to the design engineer to consider accessibility

issues in the backplane environment and plan accordingly. If this is not considered early enough in the design phase, it may not be possible to accommodate later in the project's development.

2 OVERVIEW

This paper takes a step by step look at the various design trades that need to be made when designing SpaceWire interface over a backplane. The topics covered by this paper include the following:

- Connector selection: issues to consider include choosing a connector that is suited for high reliability applications and has the appropriate characteristics for high speed signal propagation
- Impedance control: specifying a stackup and routing constraints to meet differential impedance requirements
- Signal integrity and crosstalk: impacts to the design, methods of mitigating problems, analysis tool options
- Power integrity: methods of mitigating power distribution problems, analyzing return current flow, analysis tool options
- Test and accessibility: ways of providing probing access, verifying margins, interfacing to available validation and test equipment

3 DESIGN CONSIDERATIONS

In a backplane environment, multiple cards plug into the common backplane, high speed signaling passes between cards through PCB connectors across the peripheral cards and backplane PCBs. To ensure functionality and margins, several things need to be considered as part of both the peripheral cards and backplane PCB designs.

3.1 CONNECTOR SELECTION

Connector selection is an integral part of doing design for any high speed interface, and SpaceWire is no exception. The SpaceWire standard specifies 9-pin Micro-D (MDM) connectors, cabling and shielding, however, none of these apply well to a backplane interface. Peripheral cards and backplanes typically use PCB mounted connectors, which, if not selected correctly, can result in problems ranging from unreliable operation to complete failure at the required speeds.

Rugged connectors traditionally used for backplane interface design in space flight often have high inductance/capacitance contacts which do not adequately pass high frequency signals. Additionally, the connector contacts may not be properly matched to the trace impedance, causing an impedance discontinuity which may also degrade performance. Not all vendors provide high speed propagation data for their connectors. However more and more vendors are providing this service, most often vendors whose products are commonly used for high speed applications and not for lower speed space flight applications. For the JWST and ICESAT-2 missions the backplane connectors chosen for their high speed SpaceWire applications have excellent high speed performance characteristics up to 1GHz [1]. This data was obtained from the vendor (Hypertronics Corporation) who designed these connectors for CompactPCI – another high speed application. Hypertronics makes TDR and eye pattern data readily available along with connector models for customers to use to

validate their designs by simulation. Based on their modelling, they are also able to recommend an optimal pinout for arranging the differential pairs that minimizes interfering noise. Figure 1 shows the recommended pinout and routing pattern for alternating the "+" and "-" of each differential pair within a column, separated by ground and staggered from the location of the "+" and "-" pair in the adjacent column of the connector.

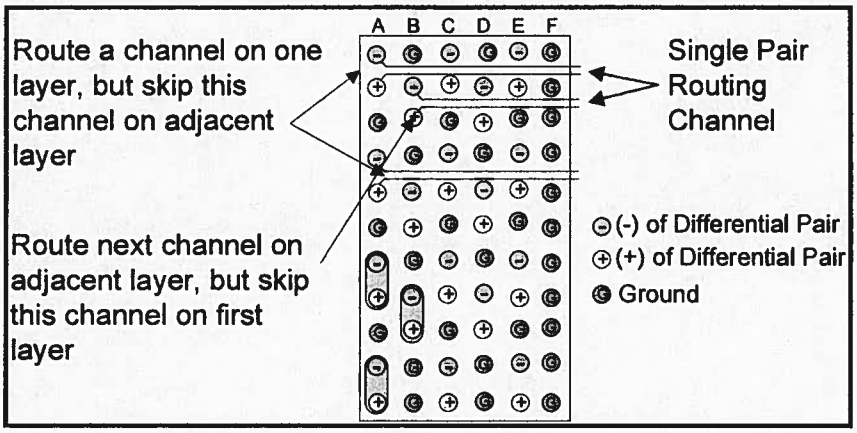

Figure 1: Connector Arrangement of a typical high density BP connector

This figure also demonstrates the difficulty with routing differential signals through the connector's pin grid. With densely spaced pins within a single connector and often multiple connectors lining up along the backplane, only a single routing channel may be routed between the pins for a single differential pair.

Connector vendors may also provide guidance on the size of the pad and antipad of the connector to reduce noise, EMI, jitter, improve manufacturability and reduce reflections that can in turn reduce data rates [2].

Designers can use various modeling tools to verify vendor data and ensure performance meets their custom requirements before locking down a design. This type of Multi-Board simulation can provide both single ended and differential simulation waveforms, along with eye pattern data [3].

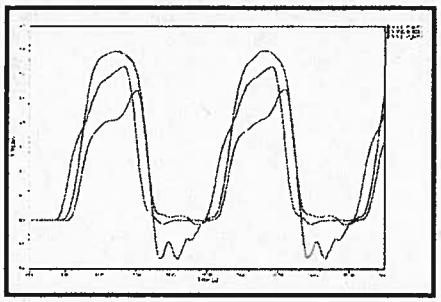

Figure 2: Differences in Signal Quality Depending on Connector Type

While all connectors make electrical connections, not all electrical connections are well suited for high speed propagation. A connector that might be qualified for flight and perfectly suitable for low edge rate signaling, may not function at the required

speeds for SpaceWire. Figure 2 shows simulated waveforms of a signal propagating between peripheral cards through a backplane using connectors with different R, L, C parasitic values. The contact R, L, C affects the path impedance and delay of the signal and can greatly change signal behaviour.

3.2 IMPEDANCE CONTROL

The electrical signaling requirements for SpaceWire over a backplane are the same as over a cabled interface, thus the 100-ohm differential impedance rule still applies. Engineers must take care to specify a set of routing rules and a PCB stackup that will meet these criteria over the entire length of the trace pair.

Figure 3 shows a typical impedance controlled stackup [3]. However, it is not enough to specify rules that meet the theoretical impedance numbers. The stackup and routing rules must also comply with a PCB vendor's manufacturing constraints. Vendors have material and process variations that mean that a set of rules that work for one vendor may not work for another and meet the same tolerances. Even with the same vendor not all materials achieve the same results. Surface finishes and the coatings used on the surface layers can change the impedance of traces routed on the outer layers. All of this must be considered upfront when choosing a vendor.

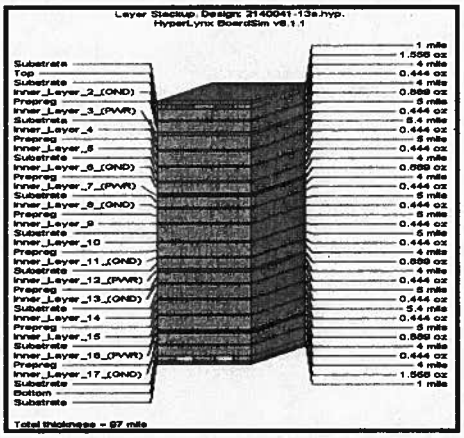

Figure 3: Example Impedance Controlled Stackup

Another trade is the differential trace routing topology. Two structures are commonly used for differential routing - edge coupled and broadside. With edge coupled, the differential pair is routed on the same layer side by side. With broadside the pair is routed on adjacent layers over-under. Figure 4 shows the difference between these two topologies. Edge coupled often presents a better solution for tighter impedance control. On the other hand, for broadside differential process and materials variations might have a larger impact on impedance variations. Vendors may not guarantee the tolerance for each broadside routing layer-pair [4].

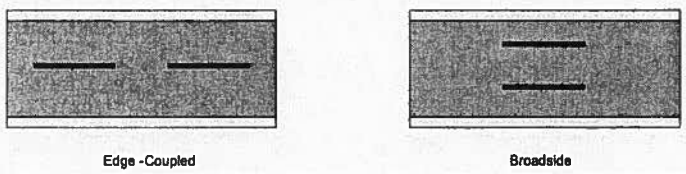

Figure 4: Edge-Coupled vs. Broadside Differential Routing

While edge-coupled may be superior for impedance control, it can be difficult to have enough space between high density connector land patterns to route a differential pair with the desired width and spacing for edge coupled impedance control as shown previously in Figure 1. This creates the need for tightly coupled differential routing, which comes with its own difficulties. Broadside routing can provide additional routing density, however depending on the di-electric thickness, may or may not create tightly coupled differential traces as well. Trades need to be made to select the appropriate structure that does not impose impossible constraints on either the design or the manufacturing process. If these things are not determined upfront, a design may not be manufacturable or may not be able to meet the 100 ohm differential impedance requirements.

3.3 Signal Integrity and Crosstalk Concerns

Signal Integrity and crosstalk concerns are not unique to SpaceWire. Any high speed PCB design has to pay special attention to ensuring proper signal integrity and minimizing crosstalk. When SpaceWire signals are not isolated by cable shielding and are routed on a backplane, they are far more susceptible to noise. This problem is exacerbated by the fact that LVDS SpaceWire signals may run on the same layer or adjacent to densely routed noisier single ended traces, such as LVTTL.

Differential traces need to be routed in a way to minimize the chance of coupling from an adjacent differential pair or an adjacent single ended trace, while at the same time maintaining the required coupling to meet differential impedance. Coupling can occur on the backplane or on the peripheral cards which source the signals or the destinations where they end. Traces run on adjacent layers, because of thin dielectric materials the separation between two signal layers might be less than a typical trace separation, causing more crosstalk than from signals routed on the same layer. Additionally, unlike in a twisted pair cable, aggressor nets can, and usually, couple asymmetrically, as opposed to common mode coupling, to each trace in the pair causing timing and jitter problems. It is important to ensure possible aggressor nets are sufficiently distant from the pair that coupling effects are insignificant.

Signal integrity can also be affected by the connector selection as mentioned earlier, the difference in trace length, and the driver or receiver devices used for the link. A practical approach to trace matching should be taken by considering the skew budget instead of trying to obtain an exact match in trace length. Adding serpentine delay lines in order to match a pair can cause more degradation of the circuit than having a practical length difference that still meets the skew budget of the fastest rise and fall times at the receiver [4].

Signal integrity analysis tools provide the best ways to trade these issues and quantify the noise risk. Eye pattern analysis can give a designer early indication of problems that might occur due to impedance mismatches or the particular type of connector and driver-receiver devices. Crosstalk can also be verified using simulation tools in a multi-board simulation environment that provides worst case numbers for coupling accumulated over the entire route. This eliminates the risk of bit failures that may only happen intermittently under certain switching situations. Corner case simulations can be used to verify margins. Figure 5 and Figure 6 show examples of simulation tool

results that designers can use to verify their designs before fabrication, avoiding costly respins and compromising mission success [3].

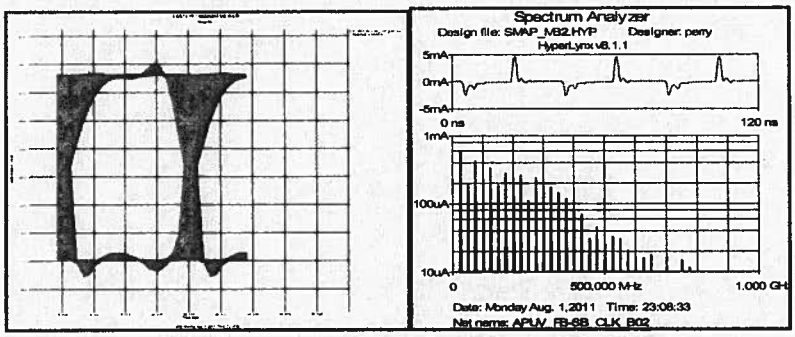

Figure 5: Example Signal Integrity/EMC Simulation Results

Type	E-Net	Receiver	Meas.	Source	Contrib
crosstalk	bp/1/net/AD21	bic/1/U1-100	354.1	AD20/bic/1/U1-104	186.9
crosstalk	bp/1/net/AD21	hk/1/U50-100	257.4	AD20/hk/1/U50-104	165.9
crosstalk	bp/1/net/AD23	bic/1/U1-94	240.3	AD21/bic/1/U1-100	161.3
crosstalk	bp/1/net/AD23	sbc/1/U1-G5	221.9	AD21/bic/1/U1-100	44.3
crosstalk	bp/1/net/AD21	sbc/1/U1-J7	217.6	AD20/bic/1/U1-104	167.5
crosstalk	bp/1/net/AD20	bic/1/U1-104	192.3	AD21/bic/1/U1-100	192.3
crosstalk	bp/1/net/AD23	fpap1/1/U1-94	182.8	AD21/hk/1/U50-100	35.7
crosstalk	bp/1/net/C_BE3_N	sbc/1/U1-J8	180.3	AD23/sbc/1/U1-G5	180.3
crosstalk	bp/1/net/AD20	hk/1/U50-104	169.5	AD21/hk/1/U50-100	169.5
crosstalk	bp/1/net/AD20	sbc/1/U1-F1	160.4	AD21/sbc/1/U1-J7	160.4
crosstalk	bp/1/net/C_BE3_N	fpap1/1/U1-86	150.3	AD23/fpap1/1/U1-94	150.3
crosstalk	bp/1/net/AD21	fpap1/1/U1-100	150.2	AD20/fpap1/1/U1-104	112.3
crosstalk	bp/1/net/AD21	fpap3/1/U1-100	148.5	AD20/bic/1/U1-104	99.2
crosstalk	bp/1/net/AD23	hk/1/U50-94	145.9	AD21/hk/1/U50-100	72.5

Figure 6: Example Crosstalk Simulation Results

3.4 POWER AND GROUND NOISE

When routing SpaceWire on a PCB, care must be taken to ensure proper routing of the ground plane as well as minimizing noise on the power delivery network (PDN). In a backplane environment there is no shielded cable that runs the differential pairs across large distances, so the shielding must be handled via ground routing on the PCB itself. Care needs to be taken to design the power distribution network where noise transients are adequately minimized. This includes having adequate decoupling capacitors but more so inter-plane capacitance that is effective at higher frequencies where decoupling capacitors are not effective. Simulations can again be used to verify PDN noise and margins.

Another important element is the location of power and return planes and the impact of return currents on inducing noise on other signals or planes. Differential traces are best routed adjacent to a ground reference plane and not crossing planes through vias, which can have unintended results with return currents and induced reverse crosstalk. This is true for the single ended signals that may share the same PCB. If care is not taken on providing for a clear return path, then unaccounted for reverse crosstalk may induce noise onto the differential signals reducing noise margins.

4 TEST AND ACCESSIBILITY

When designing backplane distribution for SpaceWire, test and accessibility considerations must be made during the design phase as access cannot be built into

the system once the PCB's are fabricated. Again, off the shelf SpaceWire test equipment is designed to interface to the standard 9 pin MDM connectors, thus without necessary access points, – test and verification when peripheral cards are installed into the backplane may prove to be impossible.

4.1 On-board Probe Access

Eye pattern measurements are a common way of verifying performance and margins. These measurements are made by attaching a differential probe near the receiver and apply to both cable and backplane based systems. If access is not designed into the PCB, optimal measurements cannot be made and the results will be inaccurate. Designers should consider placing test terminals close to the receiver in a 3 pin arrangement that complies with the dimensions of the particular model of differential probe with ground pin that will be used during testing. This makes it possible to properly connect a measurement probe without degrading the measurement. However, care must be taken that the type and placement of the test terminal will not degrade the signal itself. Modeling can again be done to ensure that the location of the terminal or the via used does not adversely affect the signal.

Another potential problem is being able to access the test terminal itself. If the card is installed into a backplane next to other cards, that that test terminal may not be accessible. During testing it may not be feasible to demate the card and test it on a bench top environment where probe access is possible or recreation of the problem may require the existence of the other cards in the system. Extender cards are an excellent way to provide access to a single card when installed in a system. However, extender card designs have to take signal and power integrity issues into consideration and may need to be custom designed for this purpose. Because adding an extender changes the trace length, any differences in propagation delay and skew must be accounted for post measurement. Multi-board simulations can again be used to validate the extender card design, and identify differences between the extender and non-extender signaling by correlating the simulated vs. actual measurement results.

4.2 Interfacing to Test Equipment and Analyzers

Test requirements often dictate the need to use link analyzers or other test equipment for functional and margin testing of the SpaceWire interface. Such equipment is likely to be available only with the standard 9 pin MDM interface. Duplicating test features with custom ground support equipment can cause an impact to schedule or be cost prohibitive. Thus ensuring that existing ground support equipment (GSE) can be used without modification is a goal designers must achieve.

One way to accomplish this is to include the footprint of a PCB mounted MDM on the peripheral card itself. However this requires additional space and may degrade the SpaceWire signals due to the location of additional stubs and vias. In this case an extender card and/or a test backplane with breakout connectors are likely to provide the best solution. In either of these conditions the unit under test is installed into the extender or test backplane. The extender or test backplane includes a breakout connector to a PCB mounted MDM connector to which test equipment can be readily connected. This offers a way to test the board in a similar arrangement to the standard cable interface without incurring any additional development cost. Figure 7 shows an

arrangement where the peripheral card backplane connector is installed on one side of a test backplane with breakout connectors on the back.

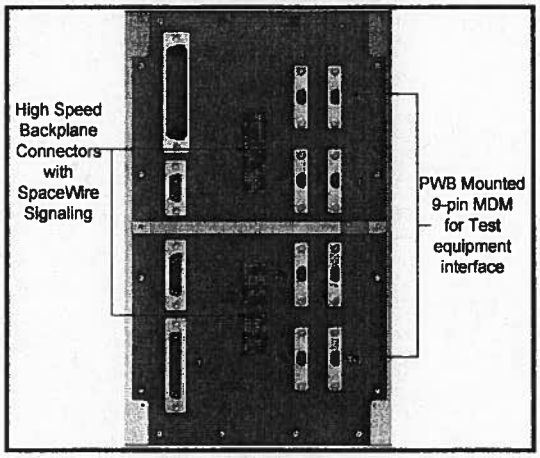

Figure 7: Peripheral Card Test Access

Designers need to accommodate the proper mechanical mounting of the PCB mounted MDM. A ground connection to the metal shell of the connector should be maintained such that the SpaceWire cable used for interfacing to the test equipment has the same grounding path as a panel mounted MDM. Without taking this into consideration it is possible to damage of degrade the flight and/or test hardware. Many PCB mounted MDM connectors do not include a metal body, so care must be taken when selecting a connector to provide proper grounding.

4.3 CONCLUSION

This paper has taken a brief look at some of the various complexities regarding a backplane distribution system for SpaceWire. While SpaceWire provides an excellent solution for board to board interfaces within a backplane distribution system, failure to consider the issues unique to this environment risk degradation of system performance, and even mission failure.

5 REFERENCES

1. Frank Morana, Hypertronics Corporation, "Single Ended and Differential TDR Characterization Data", August 2010.

2. Tyco Electronics, "AMP Z-Pack HS3 Connector Routing", Report #20GC004-1, November 15, 2000.

3. Hyperlynx SI, Hyperlynx PI and Interconnectix Synthesis, Signal and Power Integrity Tools, Mentor Graphics Inc.

4. Lee W. Ritchey, "A Treatment of Differential Signaling and its Design Requirements", Sept 9, 2008.