Block QCA Fault-Tolerant Logic Gates

It may become possible to relax manufacturing tolerances in molecular-scale devices.

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Suitably patterned arrays (blocks) of quantum-dot cellular automata (QCA) have been proposed as fault-tolerant universal logic gates. These block QCA gates could be used to realize the potential of QCA for further miniaturization, reduction of power consumption, increase in switching speed, and increased degree of integration of very-large-scale integrated (VLSI) electronic circuits.

The limitations of conventional VLSI circuitry, the basic principle of operation of QCA, and the potential advantages of QCA-based VLSI circuitry were described in several *NASA Tech Briefs* articles, namely "Implementing Permutation Matrices by Use of Quantum Dots" (NPO-20801),

Vol. 25, No. 10 (October 2001), page 42; "Compact Interconnection Networks Based on Quantum Dots" (NPO-20855) Vol. 27, No. 1 (January 2003), page 32; "Bit-Serial Adder Based on Quantum Dots" (NPO-20869), Vol. 27, No. 1 (January 2003), page 35; and "Hybrid VLSI/QCA Architecture for Computing FFTs" (NPO-20923), which follows this article. To recapitulate the principle of operation (greatly oversimplified because of the limitation on space available for this article): A quantum-dot cellular automata contains four quantum dots positioned at or between the corners of a square cell. The cell contains two extra mobile electrons that can tunnel (in the quantum-

mechanical sense) between neighboring dots within the cell. The Coulomb repulsion between the two electrons tends to make them occupy antipodal dots in the cell. For an isolated cell, there are two energetically equivalent arrangements (denoted polarization states) of the extra electrons. The cell polarization is used to encode binary information. Because the polarization of a nonisolated cell depends on Coulomb-repulsion interactions with neighboring cells, universal logic gates and binary wires could be constructed, in principle, by arraying QCA of suitable design in suitable patterns.

Heretofore, researchers have recognized two major obstacles to realization of QCA-based logic gates: One is the need for (and the difficulty of attaining) operation of QCA circuitry at room temperature or, for that matter, at any temperature above a few Kelvins. It has been theorized that room-temperature operation could be made possible by constructing QCA as molecular-scale devices. However, in approaching the lower limit of miniaturization at the molecular level, it becomes increasingly imperative to overcome the second major obstacle, which is the need for (and the difficulty of attaining) high precision in the alignments of adjacent QCA in order to ensure the correct interactions among the quantum dots.

The fault-tolerant logic gates that would be implemented by blocks of QCA according to the proposal include majority and inverter (NOT) gates, which are said to be universal logic gates because other logic gates (AND, OR, and NOR) can be implemented as combinations of majority and inverter gates. The figure depicts examples of (1) a basic QCA majority gate manufactured with exact positioning of all QCA, (2) a basic QCA majority gate manufactured with a significant position error, (3) a block QCA gate manufactured with exact positioning, and (4) a block QCA gate manufactured with irregularity of positions in the QCA array and errors in the choice of the edge QCAs used for input. These and other examples were analyzed by computational simulation, using a program developed at the University of Notre
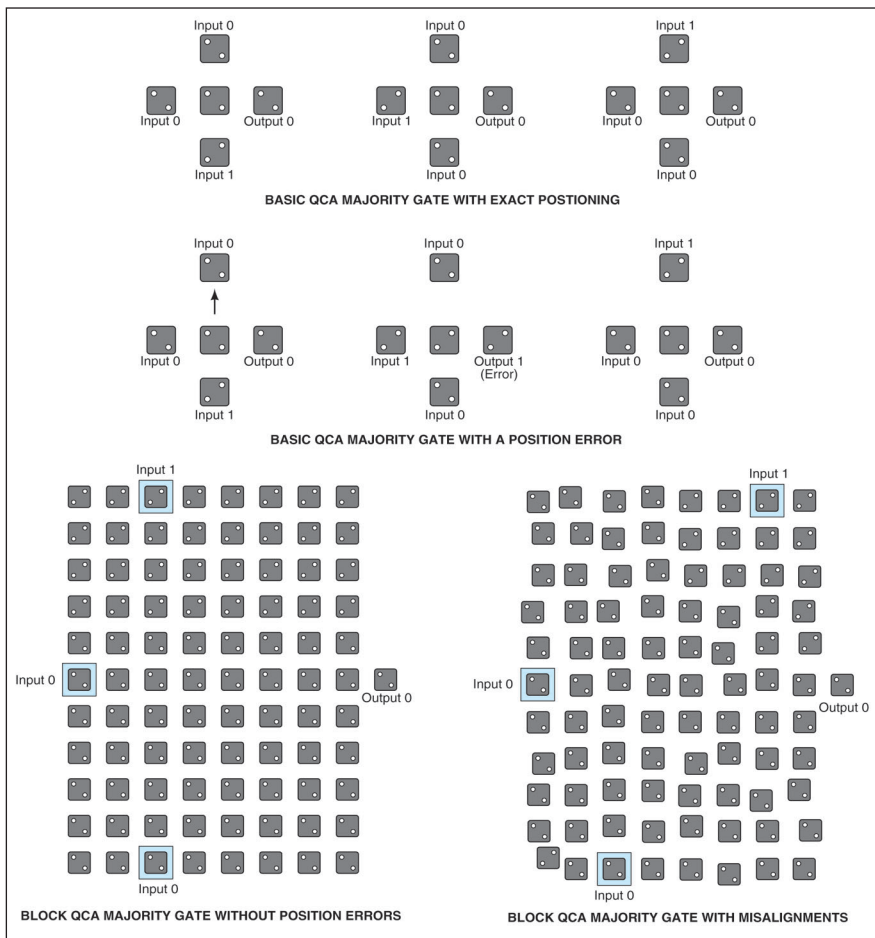
Basic and Block QCA Majority Gates, with and without misalignments, were analyzed by computational simulation. The results of the analysis showed that, relative to the basic gate, the block gate would be more tolerant of manufacturing errors.

Dame, that implements a Hartree-Fock mathematical model of the physics of a QCA array. The simulation was performed for an assumed cell size of 20 nm and inter-cell distance of 14 nm.

The results of the simulation showed that for a basic QCA majority gate, an output error would occur if the errors in the relative positions of adjacent cells were to exceed various amounts of the order of the size of a cell or a significant fraction thereof (the exact amounts being different for different cells and different directions of displacement).

In the case of a molecular implementation, this would translate to a requirement for impractical sub-nanometer manufacturing tolerances. On the other hand, the simulation showed that even with errors as large as those depicted for the block majority gate at the bottom of the figure, there would be no output error.

This work was done by Amir Firjany, Nikzad Toomarian, and Katayoon Modarres of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see Page 1).*

Hybrid VLSI/QCA Architecture for Computing FFTs
Simplification is effected through use of QCA circuitry to permute data.

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A data-processor architecture that would incorporate elements of both conventional very-large-scale integrated (VLSI) circuitry and quantum-dot cellular automata (QCA) has been proposed to enable the highly parallel and systolic computation of fast Fourier transforms (FFTs). The proposed circuit would complement the QCA-based circuits described in several prior *NASA Tech Briefs* articles, namely "Implementing Permutation Matrices by Use of Quantum Dots" (NPO-20801), Vol. 25, No. 10 (October 2001), page 42; "Compact Interconnection Networks Based on Quantum Dots" (NPO-20855) Vol. 27, No. 1 (January 2003), page 32; and "Bit-Serial Adder Based on Quantum Dots" (NPO-20869), Vol. 27, No. 1 (January 2003), page 35.

The cited prior articles described the limitations of very-large-scale integrated (VLSI) circuitry and the major potential advantage afforded by QCA. To recapitulate: In a VLSI circuit, signal paths that are required not to interact with each other must not cross in the same plane. In contrast, for reasons too complex to describe in the limited space available for this article, suitably designed and operated QCA-based signal paths that are required not to interact with each other can nevertheless be allowed to cross each other in the same plane without adverse effect. In principle, this characteristic could be exploited to design compact, coplanar, simple (relative to VLSI) QCA-based networks to implement complex, advanced interconnection schemes.
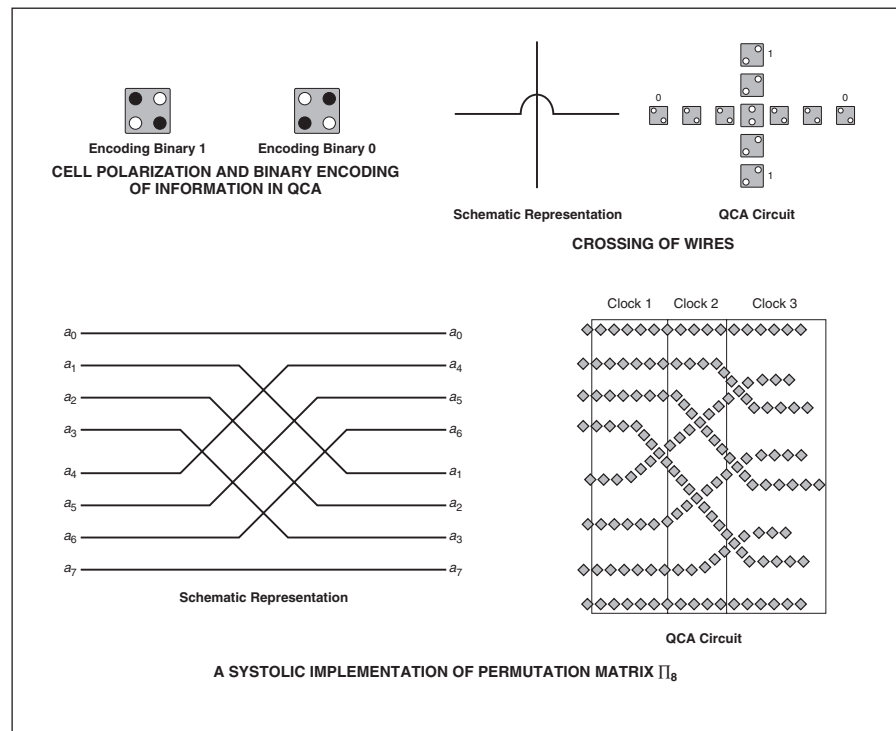

Figure 1. **QCA Are Assembled Into Binary Wires,** and the wires are patterned to implement a perfect-shuffle permutation matrix known as Π_8.

To enable a meaningful description of the proposed FFT-processor architecture, it is necessary to further recapitulate the description of a quantum-dot cellular automaton from the first-mentioned prior article: A quantum-dot cellular automaton contains four quantum dots positioned at or between the corners of a square cell. The cell contains two extra mobile electrons that can tunnel (in the quantum-mechanical sense) between neighboring dots within the cell. The Coulomb repulsion between the two electrons tends to make them occupy antipodal dots in the cell. For an isolated cell, there are two energetically equivalent arrangements (denoted polarization states) of the extra electrons. The cell polarization is used to encode binary information. Because the polarization of a nonisolated cell depends on Coulomb-repulsion interactions with neighboring cells, universal logic gates