Surface-Micromachined Planar Arrays of Thermopiles

Several design features are expected to afford improved performance.

NASA's Jet Propulsion Laboratory, Pasadena, California

Planar two-dimensional arrays of thermopiles intended for use as thermal-imaging detectors are to be fabricated by a process that includes surface micromachining. These thermopile arrays are designed to perform better than do prior two-dimensional thermopile arrays.

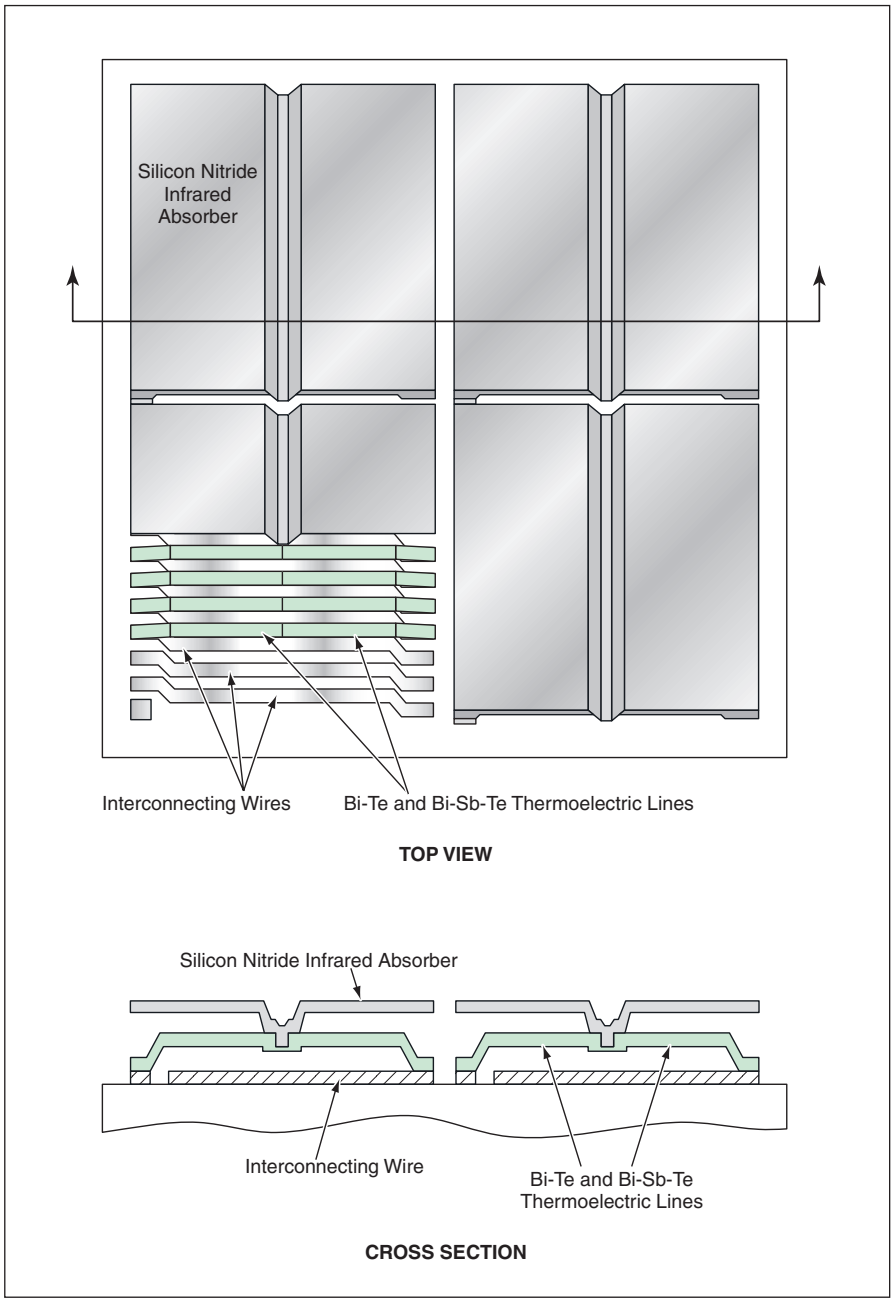
The lower performance of prior two-dimensional thermopile arrays is attributed to the following causes:

- The thermopiles are made from low-performance thermoelectric materials.
- The devices contain dielectric supporting structures, the thermal conductances of which give rise to parasitic losses of heat from detectors to substrates.
- The bulk-micromachining processes sometimes used to remove substrate material under the pixels, making it difficult to incorporate low-noise readout electronic circuitry.
- The thermoelectric lines are on the same level as the infrared absorbers, thereby reducing fill factor.

The improved pixel design of a thermopile array of the type under development is expected to afford enhanced performance by virtue of the following combination of features:

- Surface-micromachined detectors are thermally isolated through suspension above readout circuitry.
- The thermopiles are made of such high-performance thermoelectric materials as Bi-Te and Bi-Sb-Te alloys.
- Pixel structures are supported only by the thermoelectric materials: there are no supporting dielectric structures that could leak heat by conduction to the substrate.
- To maximize response, there are many thin thermoelectric legs only about 2 μm wide.
- The thermoelectric legs are hidden under a silicon nitride infrared-absorbing structure, making a large fill factor for the absorber.

The figure depicts selected aspects of four-pixel example of the improved design. The device can be characterized as a three-layer structure (or a four-layer structure if one includes the substrate). During fabrication, the device also contains two sacrificial layers, typically composed of polyimide. One sacrificial layer is located over interconnecting wires and under the thermoelectric lines; the other sacrificial layer is located over the ther-



The **Removal of Sacrificial Layers** during fabrication thermally isolates the absorber, reducing heat leaks and thereby increasing responsivity. The thinness of the thermoelectric lines and absorber makes response time short.

moelectric lines and under the silicon nitride infrared absorber. After the detector structure is fabricated, the sacrificial layers are removed, typically by etching in an oxygen plasma. The removal of the sacrificial layers is what provides the thermal isolation mentioned above.

The design facilitates maximization of the number of thermoelectric legs to increase the responsivity and the electrical impedance of the detector. Using 2-μm widths and 2-μm spacings of thermoelectric lines, it is possible to place about 11 thermocouples under a 50-μm-wide pixel.

Absorption of infrared radiation is enhanced by use of a quarter-wave cavity. In each pixel, a thin layer of metal on the silicon nitride layer constitutes a front absorber, while the thermoelectric legs and interconnecting wires, together, constitute a back-side mirror.

At the time of reporting the information for this article, partially completed detectors (lacking the silicon nitride absorbers) of 100-μm pixel size had been built and tested. The results of the test indicate a pixel resistance of 250 kΩ, responsivity of 1.5 kV/W, response time of 1.7 ms, and detectivity (D^*) of 2.4×10^8 cm·Hz$^{1/2}$/W. Improvements are ongoing.

This work was done by Marc C. Foote of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*

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Cascade Back-Propagation Learning in Neural Networks

This method would be implemented in VLSI circuitry.

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The cascade back-propagation (CBP) algorithm is the basis of a conceptual design for accelerating learning in artificial neural networks. The neural networks would be implemented as analog very-large-scale integrated (VLSI) circuits, and circuits to implement the CBP algorithm would be fabricated on the same VLSI circuit chips with the neural networks. Heretofore, artificial neural networks have learned slowly because it has been necessary to train them via software, for lack of a good on-chip learning technique. The CBP algorithm is an on-chip technique that provides for continuous learning in real time.

Artificial neural networks are trained by example: A network is presented with training inputs for which the correct outputs are known, and the algorithm strives to adjust the weights of synaptic connections in the network to make the actual outputs approach the correct outputs. The input data are generally divided into three parts. Two of the parts, called the "training" and "cross-validation" sets, respectively, must be such that the corresponding input/output pairs are known. During training, the cross-validation set enables verification of the status of the input-to-output transformation learned by the network to avoid overlearning. The third part of the data, termed the "test" set, consists of the inputs that are required to be transformed into outputs; this set may or may not include the training set and/or the cross-validation set.

Proposed neural-network circuitry for on-chip learning would be divided into two distinct networks; one for training and one for validation. Both networks would share the same synaptic weights. During training iterations, these weights would be continuously modulated according to the CBP algorithm, which is so named because it combines features of the back-propagation and cascade-correlation algorithms. Like other algorithms for learning in artificial neural networks, the CBP algorithm specifies an iterative process for adjusting the weights of synaptic connections by descent along the gradient of an error measure in the

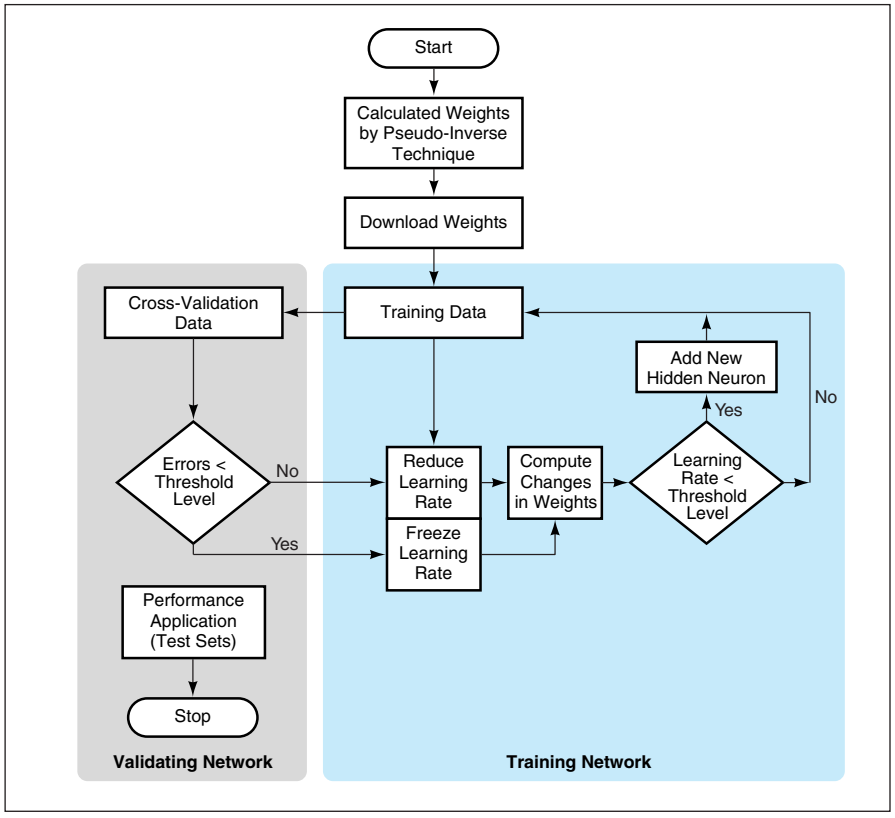

Figure 1. The **Cascade Back-Propagation Algorithm** provides the theoretical basis for design of an analog neural network that learns rapidly.