



## Capacitor-Chain Successive-Approximation ADC

This ADC could be very compact, relative to a binary-scaled successive-approximation ADC.

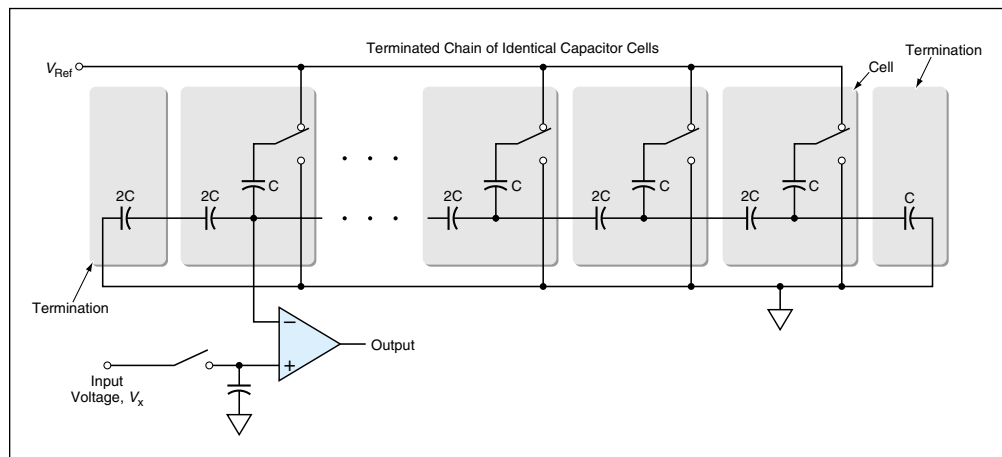
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A proposed successive-approximation analog-to-digital converter (ADC) would contain a capacitively terminated chain of identical capacitor cells (see figure). Like a conventional successive-approximation ADC containing a bank of binary-scaled capacitors, the proposed ADC would store an input voltage on a sample-and-hold capacitor and would digitize the stored input voltage by finding the closest match between this voltage and a capacitively generated sum of binary fractions of a reference voltage ( $V_{ref}$ ). However, the proposed capacitor-chain ADC would offer two major advantages over a conventional binary-scaled-capacitor ADC:

- In a conventional ADC that digitizes to  $n$  bits, the largest capacitor (representing the most significant bit) must have  $2^{n-1}$  times as much capacitance, and hence, approximately  $2^{n-1}$  times as much area as does the smallest capacitor (representing the least significant bit), so that the total capacitor area must be  $2^n$  times that of the smallest capacitor. In the proposed capacitor-chain ADC, there would be three capacitors per cell, each approximately equal to the smallest capacitor in the conventional ADC, and there would be one cell per bit. Therefore, the total capacitor area would be only about  $3n$  times that of the smallest capacitor. The net result would be that the proposed ADC could be considerably smaller than the conventional ADC.
- Because of edge effects, parasitic capacitances, and manufacturing tolerances, it is difficult to make capacitor banks in which the values of capacitance are scaled by powers of 2 to the required precision. In contrast, because all the capacitors in the proposed ADC would be identical, the problem of precise binary scaling would not arise.

In the proposed ADC, as in the conventional capacitor-chain ADC, a sampled version of the input voltage is sent together with the capacitively generated sum of binary fractions of  $V_{ref}$  into the two input terminals of a comparator. Also as in the conventional ADC, the sum of binary fractions of  $V_{ref}$  is generated by elec-

terminated to ground via capacitors of  $2C$  and  $C$ , respectively. The chain would constitute a capacitive voltage-divider network containing switched parallel and series connections. By an algebraic derivation from basic circuit theory, it can be shown that switching from the ground connection to the  $V_{ref}$  connec-



A Capacitor-Chain Successive-Approximation ADC, shown here in simplified form, would contain a capacitively terminated chain of identical capacitor cells. A sum of binary-weighted voltages would be generated by throwing switches, starting in the leftmost cell for the most-significant bit and proceeding rightward through successive cells to the least-significant bit.

tronically switching capacitor connections between ground and  $V_{ref}$ . The comparator determines whether the generated voltage is higher or lower than the input voltage, and by switching in or out successively smaller binary fractions of  $V_{ref}$ , the ADC brackets the input voltage between successively converging binary values.

Each cell could be characterized as containing two or three capacitors, depending on one's perspective: One capacitor would have the minimum capacitance,  $C$ , while the other would have a capacitance of  $2C$ . In practice, the  $2C$  capacitor could be fabricated as two  $1C$  capacitors in parallel, so that a cell would contain three identical capacitors, of which two would be tied together.

Only the first cell would be tied directly to the inverting terminal of the comparator. The second cell would be connected to the first cell, the third cell connected to the second, and so forth, forming a chain of identical cells. The first and last cells of the chain would be

tion in each successive cell of this network would contribute the next less-significant binary fraction of  $V_{ref}$  to the input terminal of the comparator. More specifically, the voltage contribution obtained by such switching in the  $m$ th cell would be given by

$$\Delta V_n = 2^{-m}(V_{ref}/3).$$

This work was done by Thomas Cunningham of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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