lines cross a given output line, only one input line is allowed to put a signal on that output line; in other words, the connections between the other input lines and the given output line are required to be of high impedance in order to block signals.

Figure 2 depicts a proposed QCA-based crosspoint switch and a 3 × 3 crossbar network. The crosspoint switch would contain several branched QCA subarrays excited by suitably phased clock signals, and one of the quantum cellular automatons would serve as a control switch. The input signal I_i would propagate toward the output line along one branch and, by suitable clocking and coupling, would be converted to another signal, I_f, propagating toward the output line along another branch. The application of a "0" signal to the control switch would cause I_i and I_f to be of the same state (both 0 or both 1), thereby causing the signal I_i to be coupled onto the output line; in effect, the crosspoint switch would be in a low-impedance state. On the other hand, the application of a "1" signal to the control switch would cause I_f to be the opposite of I_i, thereby preventing coupling of either I_i or I_f onto the output line; in effect, the crosspoint switch would be in a high-impedance state.

This work was done by Amir Fijany, Nikzad Toomarian, Katayoon Modarress, and Matthew Spotnitz of Caltech for **NASA's Jet Propulsion Laboratory**. *For further information, access the Technical Support Package (TSP)* ***free on-line at www.nasatech.com***.

NPO-20855

Laterally Coupled Quantum-Dot Distributed-Feedback Lasers

These lasers show promise for single-frequency, single-spatial mode operation.

NASA's Jet Propulsion Laboratory, Pasadena, California

InAs quantum-dot lasers that feature distributed feedback and lateral evanescent-wave coupling have been demonstrated in operation at a wavelength of 1.3 μm. These lasers are prototypes of optical-communication oscillators that are required to be capable of stable single-frequency, single-spatial-mode operation.

A laser of this type (see figure) includes an active layer that comprises multiple stacks of InAs quantum dots embedded within InGaAs quantum wells. Distributed feedback is provided by gratings formed on both sides of a ridge by electron lithography and reactive-ion etching on the surfaces of an AlGaAs/GaAs waveguide. The lateral evanescent-wave coupling between the gratings and the wave propagating in the waveguide is strong enough to ensure operation at a single frequency, and the waveguide is thick enough to sustain a stable single spatial mode.

In tests, the lasers were found to emit continuous-wave radiation at temperatures up to about 90 °C. Side modes were found to be suppressed by more than 30 dB.

This work was done by Yueming Qui, Pawan Gogna, Richard Muller, Paul Maker, and Daniel Wilson of Caltech and Andreas Stintz and Luke Lester of the University of New Mexico for **NASA's Jet Propulsion Laboratory**. *For further information, access the Technical Support Package (TSP)* ***free on-line at www.nasatech.com***.

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to

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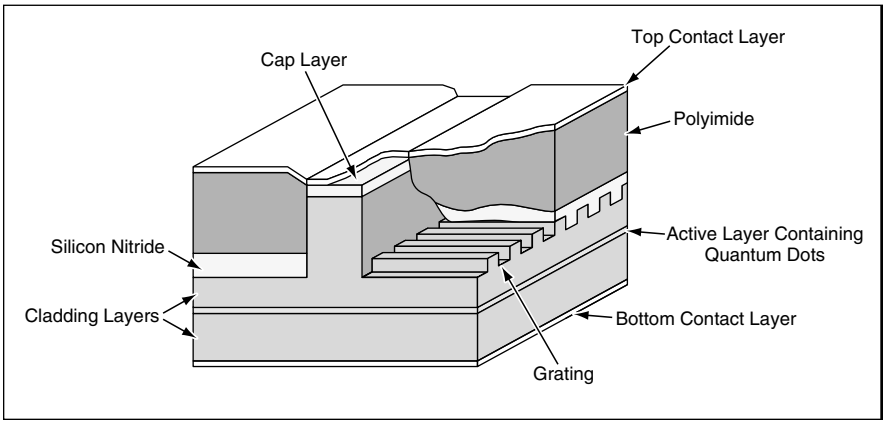
Refer to NPO-30503, volume and number of this NASA Tech Briefs *issue, and the page number.*



A **Laterally Coupled Quantum-Dot Distributed-Feedback Laser** contains structures that favor oscillation at a single frequency in a single spatial mode.

Bit-Serial Adder Based on Quantum Dots

Adders like this could be used to develop advanced, compact computers.

NASA's Jet Propulsion Laboratory, Pasadena, California

A proposed integrated circuit based on quantum-dot cellular automata (QCA) would function as a bit-serial adder. This circuit would serve as a prototype building block for demonstrating the feasibility of quantum-dots computing and for the further development of increasingly complex and increasingly capable quantum-dots computing circuits. QCA-based bit-serial adders would be especially useful in that they would enable the development of highly parallel and systolic processors for implementing fast Fourier, cosine, Hartley, and wavelet transforms.

The proposed circuit would complement the QCA-based circuits described in "Implementing Permutation Matrices by Use of Quantum Dots" (NPO-20801), *NASA Tech Briefs*, Vol. 25, No. 10 (October 2001), page 42 and "Compact Interconnection Networks Based on Quantum Dots" (NPO-20855), which appears elsewhere in this issue. Those

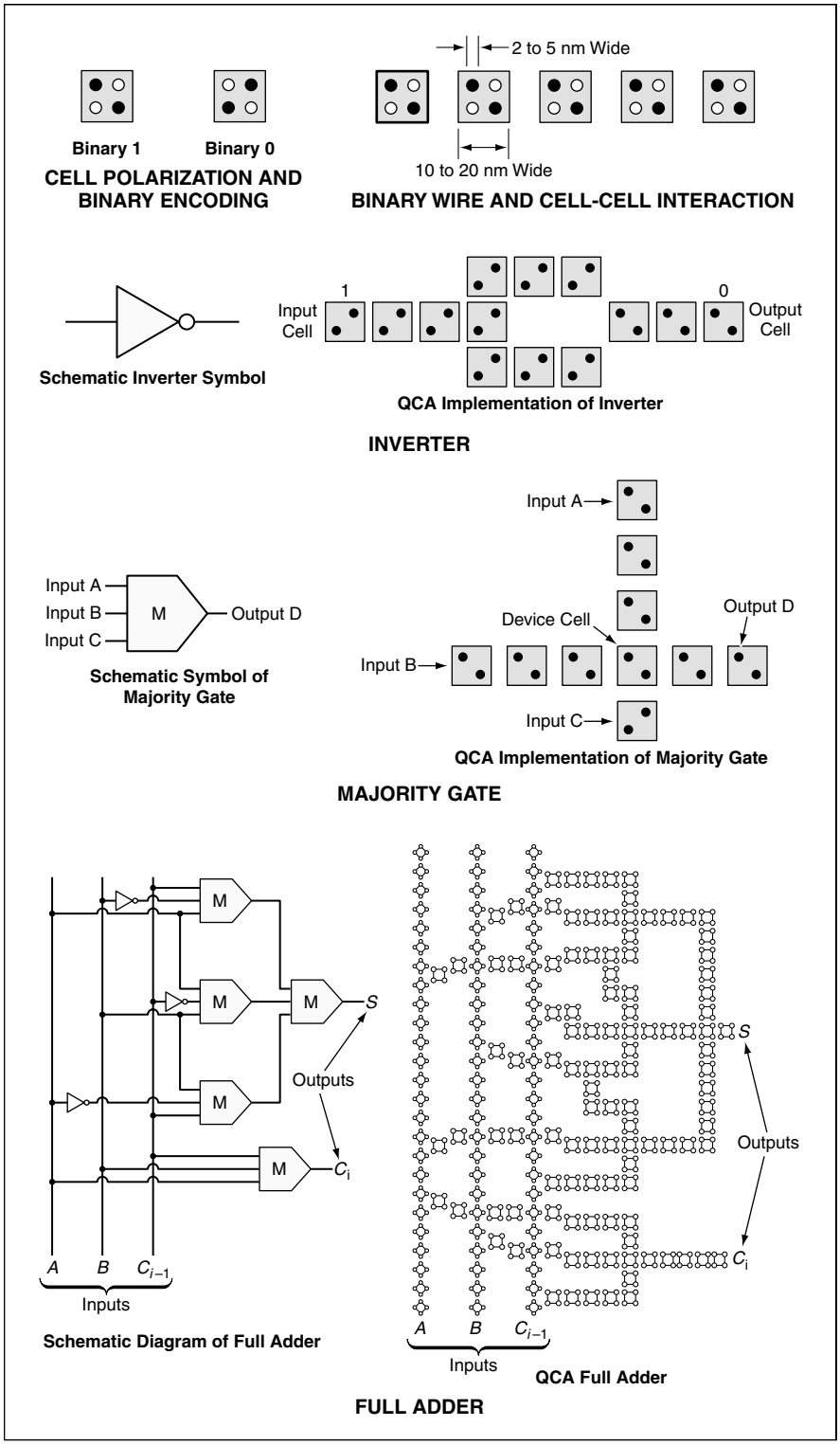


Figure 1. A **Full Adder** would be made of majority gates, inverters, and binary wires that would, in turn, be made of suitably arrayed quantum-dot cellular automata.

articles described the limitations of very-large-scale integrated (VLSI) circuitry and the major potential advantage afforded by QCA. To recapitulate: In a VLSI circuit, signal paths that are required not to interact with each other must not cross in the same plane. In contrast, for reasons too complex to describe in the limited space available for this article, suitably designed and operated QCA-based signal paths that are required not to interact with each other can nevertheless be allowed to cross each other in the same plane without adverse effect. In principle, this characteristic could be exploited to design compact, coplanar, simple (relative to VLSI) QCA-based networks to implement complex, advanced interconnection schemes.

To enable a meaningful description of the proposed bit-serial adder, it is necessary to further recapitulate the description of a quantum-dot cellular automation from the first-mentioned prior article: A quantum-dot cellular automaton contains four quantum dots positioned at the corners of a square cell. The cell contains two extra mobile electrons that can tunnel (in the quantum-mechanical sense) between neighboring dots within the cell. The Coulomb repulsion between the two electrons tends to make them occupy antipodal dots in the cell. For an isolated cell, there are two energetically equivalent arrangements (denoted polarization states) of the extra electrons. The cell polarization is used to encode binary information. Because the polarization of a nonisolated cell depends on Coulomb-repulsion interactions with neighboring cells, universal logic gates and binary wires could be constructed, in principle, by arraying QCA of suitable design in suitable patterns.

Again, for reasons too complex to describe here, in order to ensure accuracy and timeliness of the output of a QCA array, it is necessary to resort to an adiabatic switching scheme in which the QCA array is divided into subarrays, each controlled by a different phase of a multiphase clock signal. In this scheme, each subarray is given time to perform its computation, then its state is frozen by raising its interdot potential barriers and its output is fed as the input to the successor subarray. The successor subarray is kept in an unpolarized state so it does not influence the calculation of preceding subarray. Such a clocking scheme is consistent with pipeline computation in the sense that each different subarray can perform a different part of an overall computation. In other words, QCA arrays are inherently suitable for pipeline and, moreover, systolic computations. This sequential or pipeline aspect of QCA would be utilized in the proposed bit-serial adders.

The design of the proposed bit-serial adder incorporates a two-step innovation: (1) the design of an efficient QCA-based circuit that would function as a full adder, and (2) the design of QCA-based feedback loop with proper clocking that would enable the full adder to perform bit-serial addition. The full adder (see Figure 1) would contain three inverter gates and five majority gates. Given two

input bits (*A* and *B*) and one previous carry bit (C_{i-1}), this circuit would generate a sum bit (S) and a new carry bit (C_i).

A bit-serial adder would perform the addition operation on two sequences of input bits (a_i and b_i for i = 1 to n) to generate a sequence of sum bits (S_i for i = 1 to n + 1). To be able to perform the addition operation, the adder would have to be capable of storing the intermediate carry bits. A feedback loop could be used to effect such storage.

Figure 2 schematically depicts a bit-serial adder containing three majority gates and two inverter gates. This circuit could, optionally, be used as a full adder, in which role it would be more efficient, relative to the adder of Figure 1, in that it would contain fewer gates. The main advantage of the circuit of Figure 2 is that by use of suitable multiphase clocking, one could cause part of the circuit to act as a feedback loop for temporary storage of intermediate carry bits, thus enabling bit-serial addition. The ability of this circuit to perform bit-serial addition has been verified by computer simulation. However, several obstacles to practical implementation of a QCA-based bit-serial adder that could function without error at room temperature must still be overcome.

This work was done by Amir Fijany, Nikzad Toomarian, Katayoon Modarress, and Matthew Spotnitz of Caltech for **NASA's Jet Propulsion Laboratory**. *For further information, access the Technical Support Package (TSP)* ***free on-line at www.nasatech.com***.
NPO-20869

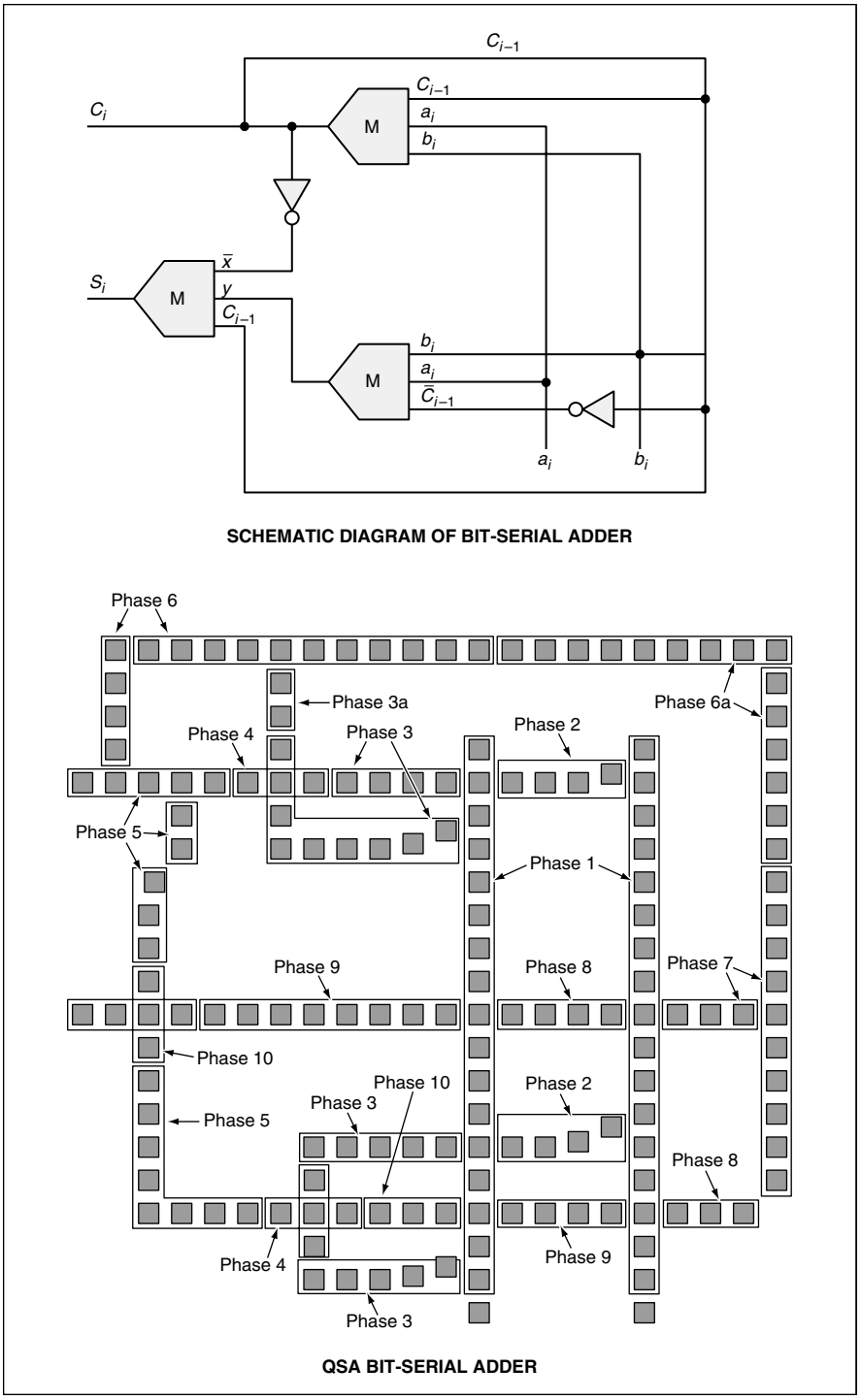


Figure 1. A **Full Adder** would be made of majority gates, inverters, and binary wires that would, in turn, be made of suitably arrayed quantum-dot cellular automata.