On-Wafer S-Parameter Measurements in the 325-508-GHz Band

NASA's Jet Propulsion Laboratory, Pasadena, California

New circuits have been designed and fabricated with operating frequencies over 325 GHz. In order to measure S-parameters of these circuits, an extensive process of wafer dicing and packaging, and waveguide transition design, fabrication, and packaging would be required. This is a costly and time-consuming process before the circuit can be tested in waveguide. The new probes and calibration procedures will simplify the testing process.

New on-wafer probes, and a procedure for their calibration, have been developed that allow fast and inexpensive S-parameter characterization of circuits in the 325-508-GHz frequency band. The on-wafer probes transition from rectangular waveguide to coplanar waveguide probe tips with 40-μm nominal signal-to-ground pin pitch so as to allow for probing circuits on a wafer. The probes with bias tees have been optimized for minimal insertion loss and maximum return loss when placed on 50-ohm structures to allow for calibration. The calibration process has been developed using the Thru-Reflect-Line Agilent algorithm with JPL determined calibration structures and calibration coefficients for the algorithm.

This new test capability is presently unique to JPL. With it, researchers will be able to better develop circuits such as low-noise amplifiers, power amplifiers, multipliers, and mixers for heterodyne receivers in the 325-508-GHz frequency band for remote sensing/spectroscopy.

This work was done by King Man Fung, Lorene A. Samoska, David M. Pukala, Douglas E. Dawson, Pekka P. Kangaslahti, Todd C. Gaier, and Charles Lawrence of Caltech; Greg Boll of GGB Industries Inc.; and Richard Lai and Xiaobing Mei of NGC for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-47575

Reconfigurable Microwave Phase Delay Element for Frequency Reference and Phase-Shifter Applications

This technology can be used in high-resolution phase shifters, frequency references, and oscillators, and in low-temperature sensors.

Goddard Space Flight Center, Greenbelt, Maryland

A technique was developed to provide a reconfigurable high-precision microwave electrical phase delay for resonators and phase shifters. The invention employs multiple branches of transmission lines with open-ended or ground-ended terminations as configurable bits or digits. This technique minimizes the errors due to limited precision of switching devices. In addition, the proposed linear analytical approach significantly produces a much simpler design than that of other prior inventions at the time of this reporting.

Microwave components such as filters, phase delay elements, or resonators require a method that can accurately adjust their frequency responses. Most tuning techniques offer very wide frequency tuning range; however, it is often difficult and expensive to tune their response in a very narrow operating frequency, especially when the tuning element reaches its minimum discrete step due to fabrication tolerances. The problem becomes worse as the operating frequency is in mm-wave frequency range (>26 GHz).

The electrical tuning sensitivity of a microwave line is dependent on the position of the tuning element with respect to the reference termination. By placing this tuning element away from this reference — with the main transmission line connecting the two elements together — the sensitivity of the tuning element can change significantly. This concept can be used in the system that requires multiple tuning sensitivities. In this case, multiple tuning branches are superimposed in the main transmission line. The proposed invention allows the transmission-line electrical length to be accurately programmed using switching elements that have limited accuracy.

The invention consists of multiple branches of transmission lines connected to discrete switching devices with open-ended terminations. They are used as discrete tuning elements. These elements are connected to the main microwave transmission line and are separated by a well-defined electrical degree spacing. Each branch is programmed to have different electrical degree sensitivity, such as a combination of discrete steps in each branch, which results in a reflective line with a unique effective phase response. To reduce the number of switching devices, it is desirable to program the devices in binary configuration where each branch represents one bit in the base-2 number system. This invention allows the transmission line electrical length to be tuned precisely with customizable sensitivity based on the known sensitivity of the base tuning circuit. The tuning resolution is dependent on the distance among tuning branches.

The novel feature of this invention is that the phase can be controlled in a very small electrical step of less than 0.5°. The sensitivity of the switching device can be scaled to minimize the errors due to fabrication process. The design technique simplifies the microwave design process. The typical microwave analysis of this device is highly non-linear and is difficult to develop in a closed-form solution. The new inven-

tion uses linear approximation technique that can accurately predict the response. Thus, the overall design process is simplified.

The conceptual model was verified with the circuit simulation, and error due to linear approximation is small and can be compensated by slightly increasing the tuning transmission line branches by a few percent. The accuracy of the theoretical model is relatively accurate, compared to the circuit model. However, the actual implementation of the invention needs to consider microwave parasitic of the switching devices and discontinuity between any microwave junctions or open-ended terminations. In addition, the absolute minimum frequency resolution is dependent on the fabrication tolerances and physical implementation of the microwave transmission lines.

This work was done by Wen-Ting Hsieh, Thomas Stevenson, Christine Jhabvala, Edward Wollack, and Kongpop U-Yen of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). ***GSC-15704-1***

High-Speed Isolation Board for Flight Hardware Testing

NASA's Jet Propulsion Laboratory, Pasadena, California

There is a need to provide a portable and cost-effective galvanic isolation between ground support equipment and flight hardware such that any unforeseen voltage differential between ground and power supplies is eliminated. An interface board was designed for use between the ground support equipment and the flight hardware that electrically isolates all input and output signals and faithfully reproduces them on each side of the interface. It utilizes highly integrated multi-channel isolating devices to minimize size and reduce assembly time.

This single-board solution provides appropriate connector hardware and breakout of required flight signals to individual connectors as needed for various ground support equipment. The board utilizes multi-channel integrated circuits that contain transformer coupling, thereby allowing input and output signals to be isolated from one another while still providing high-fidelity reproduction of the signal up to 90 MHz. The board also takes in a single-voltage power supply input from the ground support equipment and in turn provides a transformer-derived isolated voltage supply to power the portion of the circuitry that is electrically connected to the flight hardware.

Prior designs used expensive opto-isolated couplers that were required for each signal to isolate and were time-consuming to assemble. In addition, these earlier designs were bulky and required a 2U rack-mount enclosure. The new design is smaller than a piece of 8.5×11-in. (≈22×28-mm) paper and can be easily hand-carried where needed.

The flight hardware in question is based on a lineage of existing software-defined radios (SDRs) that utilize a common interface connector with many similar input-output signals present. There are currently four to five variations of this SDR, and more upcoming versions are planned based on the more recent design.

This work was done by Clifford K. Yamamoto of Caltech, and Richard L. Goodpasture of Mantech SRS Technologies for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. ***NPO-47618***

High-Throughput, Adaptive FFT Architecture for FPGA-Based Spaceborne Data Processors

This architecture can be used in digital circuit design and signal processing, and in onboard instrument data processing.

NASA's Jet Propulsion Laboratory, Pasadena, California

Exponential growth in microelectronics technology such as field-programmable gate arrays (FPGAs) has enabled high-performance spaceborne instruments with increasing onboard data processing capabilities. As a commonly used digital signal processing (DSP) building block, fast Fourier transform (FFT) has been of great interest in onboard data processing applications, which needs to strike a reasonable balance between high-performance (throughput, block size, etc.) and low resource usage (power, silicon footprint, etc.). It is also desirable to be designed so that a single design can be reused and adapted into instruments with different requirements.

The Multi-Pass Wide Kernel FFT (MPWK-FFT) architecture was developed, in which the high-throughput benefits of the parallel FFT structure and the low resource usage of Singleton's single butterfly method is exploited. The result is a wide-kernel, multipass, adaptive FFT architecture.

The 32K-point MPWK-FFT architecture includes 32 radix-2 butterflies, 64 FIFOs to store the real inputs, 64 FIFOs to store the imaginary inputs, complex twiddle factor storage, and FIFO logic to route the outputs to the correct FIFO. The inputs are stored in sequential fashion into the FIFOs, and the outputs of each butterfly are sequentially written first into the even FIFO, then the odd FIFO. Because of the order of the outputs written into the FIFOs, the depth of the even FIFOs, which are 768 each, are 1.5 times larger than the odd FIFOs, which are 512 each. The total memory needed for data storage, assuming that each sample is 36 bits, is 2.95 Mbits. The twiddle factors are stored in internal ROM inside the FPGA for fast access time. The total memory size to store the twiddle factors is 589.9Kbits.

This FFT structure combines the benefits of high throughput from the parallel FFT kernels and low resource usage