Circuit for Communication Over Power Lines

This technique can be used in vehicle sensors, building sensors, and other industrial control applications.

John H. Glenn Research Center, Cleveland, Ohio

Many distributed systems share common sensors and instruments along with a common power line supplying current to the system. A communication technique and circuit has been developed that allows for the simple inclusion of an instrument, sensor, or actuator node within any system containing a common power bus. Wherever power is available, a node can be added, which can then draw power for itself, its associated sensors, and actuators from the power bus all while communicating with other nodes on the power bus.

The technique modulates a DC power bus through capacitive coupling using on-off keying (OOK), and receives and demodulates the signal from the DC power bus through the same capacitive coupling. The circuit acts as serial modem for the physical power line communication. The circuit and technique can be made of commercially available components or included in an application specific integrated circuit (ASIC) design, which allows for the circuit to be included in current designs with additional circuitry or embedded into new designs.

This device and technique moves computational, sensing, and actuation abilities closer to the source, and allows for the networking of multiple similar nodes to each other and to a central processor. This technique also allows for reconfigurable systems by adding or removing nodes at any time. It can do so using nothing more than the *in situ* power wiring of the system.

This work was done by Michael J. Krasowski, Normal F. Prokop, Lawrence C. Greer III, and Jennifer Nappier of Glenn Research Center. Further information is contained in a TSP (see page 1).

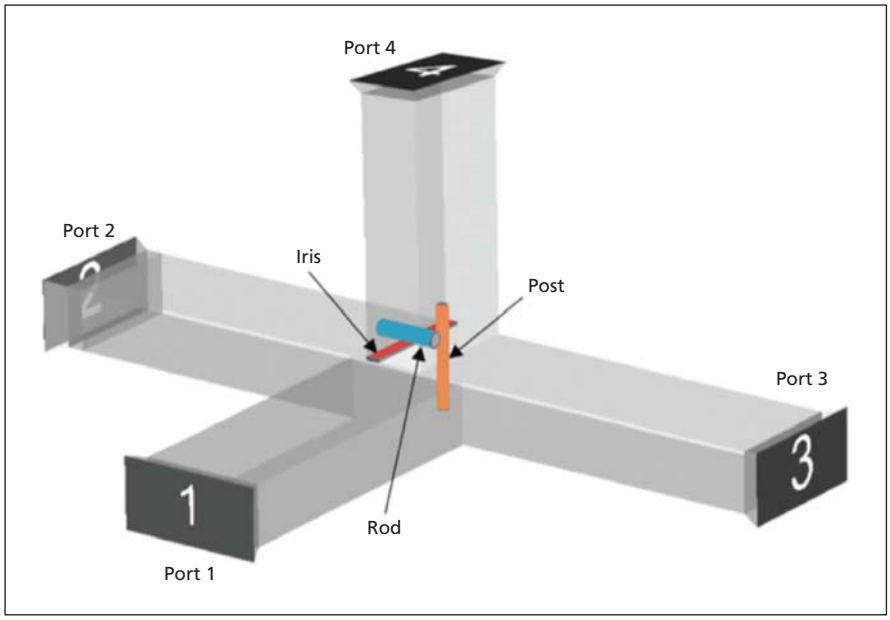
Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18631-1.

High-Efficiency Ka-Band Waveguide Two-Way Asymmetric Power Combiner

This device is applicable for use with high-power MMIC solid-state amplifiers.

John H. Glenn Research Center, Cleveland, Ohio

NASA is planning a number of Space Exploration, Earth Observation and Space Science missions where Ka-band solid-state power amplifiers (SSPAs) could have a role. Monolithic microwave integrated circuit (MMIC) based SSPAs with output powers on the order of 10 W at Ka-band frequencies would be adequate to satisfy the data transmission rate requirements at the distances involved. MMICs are a type of integrated circuit fabricated on a GaAs wafer, which operates at microwave frequencies and performs the function of signal amplification. The highest power Ka-band (31.8 to 32.3 GHz) SSPA to have flown in space had an output power of 2.6 W with an overall efficiency of 14.3 percent. This SSPA was built around discrete GaAs pHEMT (high electron mobility transistor) devices and flew aboard the Deep Space One spacecraft. State-of-the-art GaAs pHEMT-based MMIC power amplifiers (PAs) can deliver RF power at Ka-band frequencies anywhere from 3 W with a power added efficiency (PAE) of 32 percent to 6 W with a PAE of 26 percent. However, to achieve power levels higher than 6 W, the output of several MMIC PAs would need to be combined using a high-efficiency power combiner. Conventional binary waveguide power combiners, based on short-slot and magic-T circuits, require MMIC PAs with identical amplitude and phase characteristics for high combining efficiency. However, due to manufacturing process variations, the output powers of the MMIC PAs tend to be unequal, and hence the need to develop unequal power combiners.



Transparent view of **Asymmetric Combiner** showing port configuration and relative orientation of rod, post, and iris.

A two-way asymmetric magic-T based power combiner for MMIC power amplifiers, which can take in unequal inputs, has been successfully designed, fabricated, and characterized over NASA's Deep Space Network (DSN) frequency range of 31.8 to 32.3 GHz. The figure is a transparent view of the asymmetric combiner that shows the 4-port configuration and the internal structure. The rod, post, and iris are positioned by design to achieve the desired asymmetric power ratio, phase equality, and port isolation. Although the combiner was designed for an input power ratio of 2:1, it can be custom-designed for any arbitrary power ratio and frequency range. The manufactured prototype combiner was precision machined from aluminum and is less than 2 in.^{3} (32.8 cm^3). Previously investigated rectangular waveguide unequal power combiners were based on shunt/series coupling slots, E-plane septums, or H-plane T-junctions. All the prior art unequal power combiners operated at or below X-band (10 GHz) frequencies and were primarily used in the feed network of antenna arrays. The only reported asymmetric magic-T was developed as a 2:1 power divider for operation at a much lower frequency, around 500 MHz.

The measured power ratio when tested as a power divider was very close to 2 and the phase balance was within 2.6°, resulting in near ideal performance. When tested as a combiner using two MMIC SSPAs with a 2:1 power output ratio, an efficiency greater than 90 percent was demonstrated over the 500 MHz DSN frequency range. The return loss at the combiner output port (1) was greater than 18 dB and the input port (2 and 3) isolation was greater than 22 dB. The results show the asymmetric combiner to be a good candidate for high-efficiency power combining of two or more SSPAs needed to achieve the 6 to 10 W required by space communications systems of future NASA missions.

This work was done by E.G. Wintucky, R.N. Simons, and J.C. Freeman of Glenn Research Center and C.T. Chevalier of QinetiQ North America Corp. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18590-1.

10–100 Gbps Offload NIC for WAN, NLR, and Grid Computing

Goddard Space Flight Center, Greenbelt, Maryland

An extremely fast offload engine system has been developed that operates at 60 Gigabits per second (Gbps), and has scalability to 100 Gbps full-duplex (f-d). This system is based on unique coding and architecture derived from splintered UDP (User Datagram Protocol) offload technology, resulting in unique FPGA (field programmable gate array) intellectual property core and firmware.

This innovation improves the networking speed of supercomputer clusters by providing an ultra-fast network protocol processing offload from a CPU (central processing unit) by inserting an offload engine into a host backplane and network connections. This runs on protocol firmware.

This work was done by Patricia Crowley of Gonzaga University, James Awrach of SeaFire, and Arthur Maccabe of the University of New Mexico for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). *GSC-15447-1*

Pulsed Laser System to Simulate Effects of Cosmic Rays in Semiconductor Devices

The system can measure the radiation sensitivity of microelectronic devices with high spatial and temporal resolution.

NASA's Jet Propulsion Laboratory, Pasadena, California

Spaceflight system electronic devices must survive a wide range of radiation environments with various particle types including energetic protons, electrons, gamma rays, x-rays, and heavy ions. High-energy charged particles such as heavy ions can pass straight through a semiconductor material and interact with a charge-sensitive region, generating a significant amount of charge (electron-hole pairs) along their tracks. These excess charges can damage the device, and the response can range from temporary perturbations to permanent changes in the state or performance. These phenomena are called single event effects (SEE).

Before application in flight systems, electronic parts need to be qualified and tested for performance and radiation sensitivity. Typically, their susceptibility to SEE is tested by exposure to an ion beam from a particle accelerator. At such facilities, the device under test (DUT) is irradiated with large beams so there is no fine resolution to investigate particular regions of sensitivity on the parts. While it is the most reliable approach for radiation qualification, these evaluations are time consuming and costly. There is always a need for new cost-efficient strategies to complement accelerator testing: pulsed lasers provide such a solution.

Pulsed laser light can be utilized to simulate heavy ion effects with the advantage of being able to localize the sensitive region of an integrated circuit. Generally, a focused laser beam of approximately picosecond pulse duration is used to generate carrier density in the semiconductor device. During irradiation, the laser pulse is absorbed by the electronic medium with a wavelength selected accordingly by the user, and the laser energy can ionize and simulate SEE as would occur in