cell weight and volume. The composite thermal switch (CTS™) coating can be incorporated in either the anode or cathode or both. The coating can be applied in a variety of different processes that permits incorporation in the cell and electrode manufacturing processes. The CTS responds quickly and halts current flow in the hottest parts of the cell first. The coating can be applied to metal foil and supplied as a cell component onto which the active electrode materials are coated.

This work was done by Robert McDonald, Shelly Brawn, Katherine Harrison, Shannon O'Toole, and Michael Moeller of Giner, Inc. for

XMOS XC-2 Development Board for Mechanical Control and Data Collection

NASA's Jet Propulsion Laboratory, Pasadena, California

The scanning microwave limb sounder (SMLS) will use technological improvements in low-noise mixers to provide precise data on the Earth's atmospheric composition with high spatial resolution. This project focuses on the design and implementation of a real-time control system needed for airborne engineering tests of the SMLS. The system must coordinate the actuation of optical components using four motors with encoder readback, while collecting synchronized telemetric data from a GPS receiver and 3-axis gyrometric system. A graphical user interface for testing the control system was also designed using Python.

Although the system could have been implemented with an FPGA(field-programmable gate array)-based setup, a processor development kit manufactured by XMOS was chosen. The

XMOS architecture allows parallel execution of multiple tasks on separate threads, making it ideal for this application. It is easily programmed using XC (a subset of C). The necessary communication interfaces were implemented in software, including Ethernet, with significant cost and time reduction compared to an FPGA-based approach.

A simple approach to control the chopper, calibration mirror, and gimbal for the airborne SMLS was needed. The XMOS board allows for multiple threads and real-time data acquisition. The XC-2 development kit is an attractive choice for synchronized, real-time, event-driven applications. The XMOS is based on the transputer microprocessor architecture developed for parallel computing, which is being revamped in this new platform.

The XMOS device has multiple cores capable of running parallel applications on separate threads. The threads communicate with each other via user-defined channels capable of transmitting data within the device. XMOS provides a C-based development environment using XC, which eliminates the need for custom tool kits associated with FPGA programming. The XC-2 has four cores and necessary hardware for Ethernet I/O.

This work was done by Robert F. Jarnot of Caltech and William J. Bowden of the University of British Columbia for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

Receiver Gain Modulation Circuit

Applications would be in testing and development of new algorithms to detect gain anomalies and correct drifts that affect climate-quality measurements over an accelerated time scale.

Goddard Space Flight Center, Greenbelt, Maryland

A receiver gain modulation circuit (RGMC) was developed that modulates the power gain of the output of a radiometer receiver with a test signal. As the radiometer receiver switches between calibration noise references, the test signal is mixed with the calibrated noise and thus produces an ensemble set of measurements from which ensemble statistical analysis can be used to extract statistical information about the test signal. The RGMC is an enabling technology of the ensemble detector. As a key component for achieving ensemble detection and analysis, the RGMC

has broad aeronautical and space applications. The RGMC can be used to test and develop new calibration algorithms, for example, to detect gain anomalies, and/or correct for slow drifts that affect climate-quality measurements over an accelerated time scale.

A generalized approach to analyzing radiometer system designs yields a mathematical treatment of noise reference measurements in calibration algorithms. By treating the measurements from the different noise references as ensemble samples of the receiver state, i.e. receiver gain, a quantitative description of the

non-stationary properties of the underlying receiver fluctuations can be derived. Excellent agreement has been obtained between model calculations and radiometric measurements. The mathematical formulation is equivalent to modulating the gain of a stable receiver with an externally generated signal and is the basis for ensemble detection and analysis (EDA).

The concept of generating ensemble data sets using an ensemble detector is similar to the ensemble data sets generated as part of ensemble empirical mode decomposition (EEMD) with exception

of a key distinguishing factor. EEMD adds noise to the signal under study whereas EDA mixes the signal with calibrated noise. It is mixing with calibrated noise that permits the measurement of temporal-functional variability of uncertainty in the underlying process.

The RGMC permits the evaluation of EDA by modulating the receiver gain using an external signal. Without the RGMC, samples of calibrated references from radiometers form an ensemble data set of the natural occurring fluctuations within a receiver. By driving the gain of an otherwise stable receiver with an external signal, the conceptual framework and generalization of the mathematics of EDA can be tested. A series of measurements was conducted to evaluate and characterize the performance of the RGMC. Test signals stepped the RGMC across its dynamic range of performance using a radiometer that sampled four noise references; analysis indicates that the RGMC successfully modulated the receiver gain with an external signal. Calibration algorithms applied to four noise references demonstrate the RGMC produced ensemble data sets of the external signal.

NEXUS Scalable and Distributed Next-Generation Avionics Bus for Space Missions

NASA's Jet Propulsion Laboratory, Pasadena, California

A paper discusses NEXUS, a common, next-generation avionics interconnect that is transparently compatible with wired, fiber-optic, and RF physical layers; provides a flexible, scalable, packet switched topology; is fault-tolerant with sub-microsecond detection/recovery latency; has scalable bandwidth from 1 Kbps to 10 Gbps; has guaranteed real-time determinism with sub-microsecond latency/jitter; has built-in testability; features low power consumption (< 100 mW per Gbps); is lightweight with about a 5,000-logic-gate footprint; and is implemented in a small Bus Interface Unit (BIU) with reconfigurable back-end providing interface to legacy subsystems.

NEXUS enhances a commercial interconnect standard, Serial RapidIO, to meet avionics interconnect requirements without breaking the standard. This unified interconnect technology can be used to meet performance, power, size, and reliability requirements of all ranges of equipment, sensors, and actuators at chip-to-chip, board-to-board, or box-to-box boundary.

Early results from in-house modeling activity of Serial RapidIO using VisualSim indicate that the use of a switched, high-performance avionics network will provide a quantum leap in spacecraft onboard science and autonomy capability for science and exploration missions.

Digital Interface Board to Control Phase and Amplitude of Four Channels

A small set of short, high-level commands provides a simple programming interface for an external controller.

NASA's Jet Propulsion Laboratory, Pasadena, California

An increasing number of parts are designed with digital control interfaces, including phase shifters and variable attenuators. When designing an antenna array in which each antenna has independent amplitude and phase control, the number of digital control lines that must be set simultaneously can grow very large. Use of a parallel interface would require separate line drivers, more parts, and thus additional failure points. A convenient form of control where single-phase shifters or attenuators could be set or the whole set could be programmed with an update rate of 100 Hz is needed to solve this problem.

A digitial interface board with a field-programmable gate array (FPGA) can simultaneously control an essentially arbitrary number of digital control lines with a serial command interface requiring only three wires. A small set of short, high-level commands provides a simple programming interface for an external controller. Parity bits are used to validate the control commands. Output timing is controlled within the FPGA to allow for rapid update rates of the phase shifters and attenuators.

This technology has been used to set and monitor eight 5-bit control signals via a serial UART (universal asynchronous receiver/transmitter) interface. The digital interface board controls the phase and amplitude of the signals for each element in the array. A host computer running Agilent VEE sends commands via serial UART connection to a Xilinx VirtexII FPGA. The commands are decoded, and either outputs are set or telemetry data is sent back to the host computer describing the status and the current phase and amplitude settings.

This technology is an integral part of a closed-loop system in which the angle of arrival of an X-band uplink signal is detected and the appropriate phase shifts are applied to the Ka-band downlink signal to electronically steer the array back in the direction of the