uplink signal. It will also be used in the non-beam-steering case to compensate for phase shift variations through power amplifiers. The digital interface board can be used to set four 5-bit phase shifters and four 5-bit attenuators and monitor their current settings. Additionally, it is useful outside of the closed-loop system for beam-steering alone.

When the VEE program is started, it prompts the user to initialize variables (to zero) or skip initialization. After that, the program enters into a continuous loop waiting for the telemetry period to elapse or a button to be pushed. A telemetry request is sent when the telemetry period is elapsed (every five seconds). Pushing one of the set or reset buttons will send the appropriate command. When a command is sent, the interface status is returned, and the user will be notified by a pop-up window if any error has occurred. The program runs until the End Program button is depressed.

This work was done by Amy E. Smith, Brian M. Cook, Abdur R. Khan, and James P. Lux of Caltech, for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov.

This software is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. Refer to NPO-42778.

CoNNeCT Baseband Processor Module

Goddard Space Flight Center, Greenbelt, Maryland

A document describes the CoNNeCT Baseband Processor Module (BPM) based on an updated processor, memory technology, and field-programmable gate arrays (FPGAs). The BPM was developed from a requirement to provide sufficient computing power and memory storage to conduct experiments for a Software Defined Radio (SDR) to be implemented.

The flight SDR uses the AT697 SPARC processor with on-chip data and instruction cache. The non-volatile memory has been increased from a 20-Mbit EEPROM (electrically erasable programmable read only memory) to a 4-Gbit Flash, managed by the RTAX2000 Housekeeper, allowing more programs and FPGA bit-files to be stored. The volatile memory has been increased from a 20-Mbit SRAM (static random access memory) to a 1.25-Gbit SDRAM (synchronous dynamic random access memory), providing additional memory space for more complex operating systems and programs to be executed on the SPARC. All memory is EDAC (error detection and correction) protected, while the SPARC processor implements fault protection via TMR (triple modular redundancy) architecture.

Further capability over prior BPM designs includes the addition of a second FPGA to implement features beyond the resources of a single FPGA. Both FPGAs are implemented with Xilinx Virtex-II and are interconnected by a 96-bit bus to facilitate data exchange. Dedicated 1.25-Gbit SDRAMs are wired to each Xilinx FPGA to accommodate high rate data buffering for SDR applications as well as independent SpaceWire interfaces. The RTAX2000 manages scrub and configuration of each Xilinx.

This work was done by Clifford K. Yamamoto, Thomas C. Jedrey, and Daniel G. Gutrich of Caltech, and Richard L. Goodpasture of Mantech SRS Technologies for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). **NPO-47773**

Cryogenic 160-GHz MMIC Heterodyne Receiver Module

Applications include portable security sensors, hidden weapons detection, airport security, and automotive radar.

NASA's Jet Propulsion Laboratory, Pasadena, California

A cryogenic 160-GHz MMIC heterodyne receiver module has demonstrated a system noise temperature of 100 K or less at 166 GHz. This module builds upon work previously described in "Development of a 150-GHz MMIC Module Prototype for Large-Scale CMB Radiation" (NPO-47664), *NASA Tech Briefs*, Vol. 35, No. 8 (August 2011), p. 27. In the original module, the local oscillator signal was saturating the MMIC low-noise amplifiers (LNAs) with power. In order to suppress the local oscillator signal from reaching the MMIC LNAs, the W-band (75–110 GHz) signal had to be filtered out before reaching 140–170 GHz. A bandpass filter was developed to cover 120–170 GHz, using microstrip parallel-coupled lines to achieve the desired filter bandwidth, and ensure that the unwanted W-band local oscillator signal would be sufficiently suppressed.

With the new bandpass filter, the entire receiver can work over the 140–180-GHz band, with a minimum system noise temperature of 460 K at 166 GHz. The module was tested cryogenically at 20 K ambient temperature, and it was found that the receiver had a noise temperature of 100 K over an 8-GHz bandwidth.

The receiver module now includes a microstrip bandpass filter, which was designed to have a 3-dB bandwidth of approximately 120–170 GHz. The filter was fabricated on a 3-mil-thick alumina substrate. The filter design was based on a W-band filter design made at JPL and used in the QUIET (Q/U Imaging ExperimenT) radiometer modules. The W-band filter was scaled for a new center frequency of 150 GHz, and the microstrip segments were changed accordingly. Also, to decrease the bandwidth of the resulting scaled design, the center gaps between the microstrip lines were increased (by four micrometers in length) compared to the gaps near the edges.

The use of the 150-GHz bandpass filter has enabled the receiver module to function well at room temperature. The system noise temperature was measured to be less than 600 K (at room temperature) from 154 to 168 GHz. Additionally, the use of a W-band isolator between the receiver module and the local oscillator source also