of a key distinguishing factor. EEMD adds noise to the signal under study whereas EDA mixes the signal with calibrated noise. It is mixing with calibrated noise that permits the measurement of temporal-functional variability of uncertainty in the underlying process.

The RGMC permits the evaluation of EDA by modulating the receiver gain using an external signal. Without the RGMC, samples of calibrated references from radiometers form an ensemble data set of the natural occurring fluctuations within a receiver. By driving the gain of an otherwise stable receiver with an external signal, the conceptual framework and generalization of the mathematics of EDA can be tested. A series of measurements was conducted to evaluate and characterize the performance of the RGMC. Test signals stepped the RGMC across its dynamic range of performance using a radiometer that sampled four noise references; analysis indicates that the RGMC successfully modulated the receiver gain with an external signal. Calibration algorithms applied to four noise references demonstrate the RGMC produced ensemble data sets of the external signal.

NEXUS Scalable and Distributed Next-Generation Avionics Bus for Space Missions

NASA's Jet Propulsion Laboratory, Pasadena, California

A paper discusses NEXUS, a common, next-generation avionics interconnect that is transparently compatible with wired, fiber-optic, and RF physical layers; provides a flexible, scalable, packet switched topology; is fault-tolerant with sub-microsecond detection/recovery latency; has scalable bandwidth from 1 Kbps to 10 Gbps; has guaranteed real-time determinism with sub-microsecond latency/jitter; has built-in testability; features low power consumption (< 100 mW per Gbps); is lightweight with about a 5,000-logic-gate footprint; and is implemented in a small Bus Interface Unit (BIU) with reconfigurable back-end providing interface to legacy subsystems.

NEXUS enhances a commercial interconnect standard, Serial RapidIO, to meet avionics interconnect requirements without breaking the standard. This unified interconnect technology can be used to meet performance, power, size, and reliability requirements of all ranges of equipment, sensors, and actuators at chip-to-chip, board-to-board, or box-to-box boundary.

Early results from in-house modeling activity of Serial RapidIO using VisualSim indicate that the use of a switched, high-performance avionics network will provide a quantum leap in spacecraft onboard science and autonomy capability for science and exploration missions.

Digital Interface Board to Control Phase and Amplitude of Four Channels

A small set of short, high-level commands provides a simple programming interface for an external controller.

NASA's Jet Propulsion Laboratory, Pasadena, California

An increasing number of parts are designed with digital control interfaces, including phase shifters and variable attenuators. When designing an antenna array in which each antenna has independent amplitude and phase control, the number of digital control lines that must be set simultaneously can grow very large. Use of a parallel interface would require separate line drivers, more parts, and thus additional failure points. A convenient form of control where single-phase shifters or attenuators could be set or the whole set could be programmed with an update rate of 100 Hz is needed to solve this problem.

A digitial interface board with a field-programmable gate array (FPGA) can simultaneously control an essentially arbitrary number of digital control lines with a serial command interface requiring only three wires. A small set of short, high-level commands provides a simple programming interface for an external controller. Parity bits are used to validate the control commands. Output timing is controlled within the FPGA to allow for rapid update rates of the phase shifters and attenuators.

This technology has been used to set and monitor eight 5-bit control signals via a serial UART (universal asynchronous receiver/transmitter) interface. The digital interface board controls the phase and amplitude of the signals for each element in the array. A host computer running Agilent VEE sends commands via serial UART connection to a Xilinx VirtexII FPGA. The commands are decoded, and either outputs are set or telemetry data is sent back to the host computer describing the status and the current phase and amplitude settings.

This technology is an integral part of a closed-loop system in which the angle of arrival of an X-band uplink signal is detected and the appropriate phase shifts are applied to the Ka-band downlink signal to electronically steer the array back in the direction of the

uplink signal. It will also be used in the non-beam-steering case to compensate for phase shift variations through power amplifiers. The digital interface board can be used to set four 5-bit phase shifters and four 5-bit attenuators and monitor their current settings. Additionally, it is useful outside of the closed-loop system for beam-steering alone.

When the VEE program is started, it prompts the user to initialize variables (to zero) or skip initialization. After that, the program enters into a continuous loop waiting for the telemetry period to elapse or a button to be pushed. A telemetry request is sent when the telemetry period is elapsed (every five seconds). Pushing one of the set or reset buttons will send the appropriate command. When a command is sent, the interface status is returned, and the user will be notified by a pop-up window if any error has occurred. The program runs until the End Program button is depressed.

CoNNeCT Baseband Processor Module

Goddard Space Flight Center, Greenbelt, Maryland

A document describes the CoNNeCT Baseband Processor Module (BPM) based on an updated processor, memory technology, and field-programmable gate arrays (FPGAs). The BPM was developed from a requirement to provide sufficient computing power and memory storage to conduct experiments for a Software Defined Radio (SDR) to be implemented.

The flight SDR uses the AT697 SPARC processor with on-chip data and instruction cache. The non-volatile memory has been increased from a 20-Mbit EEPROM (electrically erasable programmable read only memory) to a 4-Gbit Flash, managed by the RTAX2000 Housekeeper, allowing more programs and FPGA bit-files to be stored. The volatile memory has been increased from a 20-Mbit SRAM (static random access memory) to a 1.25-Gbit SDRAM (synchronous dynamic random access memory), providing additional memory space for more complex operating systems and programs to be executed on the SPARC. All memory is EDAC (error detection and correction) protected, while the SPARC processor implements fault protection via TMR (triple modular redundancy) architecture.

Further capability over prior BPM designs includes the addition of a second FPGA to implement features beyond the resources of a single FPGA. Both FPGAs are implemented with Xilinx Virtex-II and are interconnected by a 96-bit bus to facilitate data exchange. Dedicated 1.25-Gbit SDRAMs are wired to each Xilinx FPGA to accommodate high rate data buffering for SDR applications as well as independent SpaceWire interfaces. The RTAX2000 manages scrub and configuration of each Xilinx.

Cryogenic 160-GHz MMIC Heterodyne Receiver Module
Applications include portable security sensors, hidden weapons detection, airport security, and automotive radar.

NASA's Jet Propulsion Laboratory, Pasadena, California

A cryogenic 160-GHz MMIC heterodyne receiver module has demonstrated a system noise temperature of 100 K or less at 166 GHz. This module builds upon work previously described in "Development of a 150-GHz MMIC Module Prototype for Large-Scale CMB Radiation" (NPO-47664), *NASA Tech Briefs*, Vol. 35, No. 8 (August 2011), p. 27. In the original module, the local oscillator signal was saturating the MMIC low-noise amplifiers (LNAs) with power. In order to suppress the local oscillator signal from reaching the MMIC LNAs, the W-band (75–110 GHz) signal had to be filtered out before reaching 140–170 GHz. A bandpass filter was developed to cover 120–170 GHz, using microstrip parallel-coupled lines to achieve the desired filter bandwidth, and ensure that the unwanted W-band local oscillator signal would be sufficiently suppressed.

With the new bandpass filter, the entire receiver can work over the 140–180-GHz band, with a minimum system noise temperature of 460 K at 166 GHz. The module was tested cryogenically at 20 K ambient temperature, and it was found that the receiver had a noise temperature of 100 K over an 8-GHz bandwidth.

The receiver module now includes a microstrip bandpass filter, which was designed to have a 3-dB bandwidth of approximately 120–170 GHz. The filter was fabricated on a 3-mil-thick alumina substrate. The filter design was based on a W-band filter design made at JPL and used in the QUIET (Q/U Imaging ExperimenT) radiometer modules. The W-band filter was scaled for a new center frequency of 150 GHz, and the microstrip segments were changed accordingly. Also, to decrease the bandwidth of the resulting scaled design, the center gaps between the microstrip lines were increased (by four micrometers in length) compared to the gaps near the edges.

The use of the 150-GHz bandpass filter has enabled the receiver module to function well at room temperature. The system noise temperature was measured to be less than 600 K (at room temperature) from 154 to 168 GHz. Additionally, the use of a W-band isolator between the receiver module and the local oscillator source also