



## Books & Reports

### **Rad-Hard, Miniaturized, Scalable, High-Voltage Switching Module for Power Applications**

A paper discusses the successful development of a miniaturized radiation hardened high-voltage switching module operating at 2.5 kV suitable for space application. The high-voltage architecture was designed, fabricated, and tested using a commercial process that uses a unique combination of 0.25  $\mu\text{m}$  CMOS (complementary metal oxide semiconductor) transistors and high-voltage lateral DMOS (diffusion metal oxide semiconductor) device with high breakdown voltage (>650 V). The high-voltage requirements are achieved by stacking a number of DMOS devices within one module, while two modules can be placed in series to achieve higher voltages.

Besides the high-voltage requirements, a second generation prototype is currently being developed to provide improved switching capabilities (rise time and fall time for full range of target voltages and currents), the ability to scale the output voltage to a desired value with good accuracy (few percent) up to 10 kV, to cover a wide range of high-voltage applications. In addition, to ensure miniaturization, long life, and high reliability, the assemblies will require intensive high-voltage electrostatic modeling (opti-

mized E-field distribution throughout the module) to complete the proposed packaging approach and test the applicability of using advanced materials in a space-like environment (temperature and pressure) to help prevent potential arcing and corona due to high field regions.

Finally, a single-event effect evaluation would have to be performed and single-event mitigation methods implemented at the design and system level or developed to ensure complete radiation hardness of the module.

*This work was done by Philippe C. Adell, Mohammad Mojarradi, Linda Y. Del Castillo, and Tuan A. Vo of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47784*

### **Architecture for a 1-GHz Digital RADAR**

An architecture for a Direct RF-digitization Type Digital Mode RADAR was developed at GSFC in 2008. Two variations of a basic architecture were developed for use on RADAR imaging missions using aircraft and spacecraft. Both systems can operate with a pulse repetition rate up to 10 MHz with 8 received RF samples per pulse repetition interval, or at up to 19 kHz with 4K received RF samples per pulse repetition interval.

The first design describes a computer architecture for a Continuous Mode RADAR transceiver with a real-time sig-

nal processing and display architecture. The architecture can operate at a high pulse repetition rate without interruption for an infinite amount of time. The second design describes a smaller and less costly burst mode RADAR that can transceive high pulse repetition rate RF signals without interruption for up to 37 seconds. The burst-mode RADAR was designed to operate on an off-line signal processing paradigm.

The temporal distribution of RF samples acquired and reported to the RADAR processor remains uniform and free of distortion in both proposed architectures. The majority of the RADAR's electronics is implemented in digital CMOS (complementary metal oxide semiconductor), and analog circuits are restricted to signal amplification operations and analog to digital conversion.

An implementation of the proposed systems will create a 1-GHz, Direct RF-digitization Type, L-Band Digital RADAR — the highest band achievable for Nyquist Rate, Direct RF-digitization Systems that do not implement an electronic IF downsample stage (after the receiver signal amplification stage), using commercially available off-the-shelf integrated circuits.

*This work was done by Udayan Mallik at Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15716-1*