
Cable Tester Box

NASA's Jet Propulsion Laboratory, Pasadena, California

Cables are very important electrical devices that carry power and signals across multiple instruments. Any fault in a cable can easily result in a catastrophic outcome. Therefore, verifying that all cables are built to spec is a very important part of Electrical Integration Procedures. Currently, there are two methods used in lab for verifying cable connectivity. (1) Using a Break-Out Box and an ohmmeter — this method is time-consuming but effective for custom cables — and (2) Commercial Automated Cable Tester Boxes — this method is fast, but to test custom cables often requires pre-programmed configuration files, and cables used on spacecraft are often uniquely designed for specific purposes.

The idea is to develop a semi-automatic continuity tester that reduces

human effort in cable testing, speeds up the electrical integration process, and ensures system safety.

The JPL-Cable Tester Box is developed to check every single possible electrical connection in a cable in parallel. This system indicates connectivity through LED (light emitting diode) circuits. Users can choose to test any pin/shell (test node) with a single push of a button, and any other nodes that are shorted to the test node, even if they are in the same connector, will light up with the test node.

The JPL-Cable Tester Boxes offers the following advantages:

1. Easy to use: The architecture is simple enough that it only takes 5 minutes for anyone to learn how operate the Cable Tester Box. No pre-pro-

gramming and calibration are required, since this box only checks continuity.

2. Fast: The cable tester box checks all the possible electrical connections in parallel at a push of a button. If a cable normally takes half an hour to test, using the Cable Tester Box will improve the speed to as little as 60 seconds to complete.

3. Versatile: Multiple cable tester boxes can be used together. As long as all the boxes share the same electrical potential, any number of connectors can be tested together.

This work was done by Jason H. Lee of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-46800

Programmable Oscillator

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A programmable oscillator is a frequency synthesizer with an output phase that tracks an arbitrary function. An offset, phase-locked loop circuit is used in combination with an error control feedback loop to precisely control the output phase of the oscillator.

To down-convert the received signal, several stages of mixing may be employed with the compensation for the time-base distortion of the carrier occur-

ring at any one of those stages. In the Goldstone Solar System Radar (GSSR), the compensation occurs in the mixing from an intermediate frequency (IF), whose value is dependent on the station and band, to a common IF used in the final stage of down-conversion to baseband. The programmable oscillator (PO) is used in the final stage of down-conversion to generate the IF, along with a time-varying phase component that

matches the time-base distortion of the carrier, thus removing it from the final down-converted signal.

This work was done by Kevin J. Quirk, Ferze D. Patawaran, Danh H. Nguyen, and Clement G. Lee of Caltech and Huy Nguyen for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47657

Fault-Tolerant, Radiation-Hard DSP

This technology can be applied to commercial communications and GPS satellites.

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Commercial digital signal processors (DSPs) for use in high-speed satellite computers are challenged by the damaging effects of space radiation, mainly single event upsets (SEUs) and single event functional interrupts (SEFIs). Innovations have been developed for mitigating the effects of SEUs and SEFIs, enabling the use of very-high-speed commercial DSPs with improved SEU tolerances. Time-triple modular redundancy (TTMR) is a method of applying traditional triple modular redun-

dancy on a single processor, exploiting the VLIW (very long instruction word) class of parallel processors. TTMR improves SEU rates substantially. SEFIs are solved by a SEFI-hardened core circuit, external to the microprocessor. It monitors the "health" of the processor, and if a SEFI occurs, forces the processor to return to performance through a series of escalating events.

TTMR and hardened-core solutions were developed for both DSPs and reconfigurable field-programmable gate

arrays (FPGAs). This includes advancement of TTMR algorithms for DSPs and reconfigurable FPGAs, plus a rad-hard, hardened-core integrated circuit that services both the DSP and FPGA. Additionally, a combined DSP and FPGA board architecture was fully developed into a rad-hard engineering product. This technology enables use of commercial off-the-shelf (COTS) DSPs in computers for satellite and other space applications, allowing rapid deployment at a much lower cost.