Improvements in Speed and Functionality of a 670-GHz Imaging Radar

Image acquisition time has been reduced, enabling clearer images of contraband objects hidden underneath clothing.

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Significant improvements have been made in the instrument originally described in a prior *NASA Tech Briefs* article: "Improved Speed and Functionality of a 580-GHz Imaging Radar" (NPO-45156), Vol. 34, No. 7 (July 2010), p. 51. First, the wideband YIG oscillator has been replaced with a JPL-designed and built phase-locked, low-noise chirp source. Second, further refinements to the data acquisition and signal processing software have been performed by moving critical code sections to C code, and compiling those sections to Windows DLLs, which are then invoked from the main LabVIEW executive.

This system is an active, single-pixel scanned imager operating at 670 GHz. The actual chirp signals for the RF and LO chains were generated by a pair of MITEQ 2.5–3.3 GHz chirp sources. Agilent benchtop synthesizers operating at fixed frequencies around 13 GHz were then used to up-convert the chirp sources to 15.5–16.3 GHz. The resulting signals were then multiplied 36 times by a combination of off-the-shelf millimeter-wave components, and JPL-built 200-GHz doublers and 300- and 600-GHz triplers. The power required to drive the submillimeter-wave multipliers was provided by JPL-built W-band amplifiers. The receive and transmit signal paths were combined using a thin, high-resistivity silicon wafer as a beam splitter.

While the results at present are encouraging, the system still lacks sufficient speed to be usable for practical applications in a contraband detection. Ideally, an image acquisition speed of ten seconds, or a factor of 30 improvement, is desired. However, the system improvements to date have resulted in a factor of five increase in signal acquisition speed, as well as enhanced signal-processing algorithms, permitting clearer imaging of contraband objects hidden underneath clothing. In particular, advances in three distinct areas have enabled these performance enhancements: base source phase noise reduction, chirp rate, and signal processing. Additionally, a second pixel was added, automatically reducing the imaging time by a factor of two. Although adding a second pixel to the system doubles the amount of submillimeter components required, some savings in microwave hardware can be realized by using a common low-noise source.

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In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-47180, volume and number of this NASA Tech Briefs *issue, and the page number.*

IONAC-Lite

A combination of energy and performance optimization is attained for high-speed Delay Tolerant Networking.

NASA's Jet Propulsion Laboratory, Pasadena, California

The Interplanetary Overlay Networking Protocol Accelerator (IONAC) described previously in "The Interplanetary Overlay Networking Protocol Accelerator" (NPO-45584), *NASA Tech Briefs*, Vol. 32, No. 10, (October 2008) p. 106 (*http://www.techbriefs.com/component/content/article/3317*) provides functions that implement the Delay Tolerant Networking (DTN) bundle protocol. New missions that require high-speed downlink-only use of DTN can now be accommodated by the unidirectional IONAC-Lite to support high data rate downlink mission applications. Due to constrained energy resources, a conventional software implementation of the DTN protocol can provide only limited throughput for any given reasonable energy consumption rate. The IONAC-Lite DTN Protocol Accelerator is able to reduce this energy consumption by an order of magnitude and increase the throughput capability by two orders of magnitude. In addition, a conventional DTN implementation requires a bundle database with a considerable storage requirement. In very high downlink data-rate missions such as near-Earth radar science missions, the storage space utilization needs to be maximized for science data and minimized for communications protocol-related storage needs.

The IONAC-Lite DTN Protocol Accelerator is implemented in a reconfigurable hardware device to accomplish exactly what's needed for high-throughput DTN downlink-only scenarios.

The following are salient features of the IONAC-Lite implementation:

• An implementation of the Bundle Pro-