Frequency to Voltage Converter Analog Front-End Prototype

The device compares multiple filter circuits side-by-side.

John F. Kennedy Space Center, Florida

The frequency to voltage converter analog front end evaluation prototype (F2V AFE) is an evaluation board designed for comparison of different methods of accurately extracting the frequency of a sinusoidal input signal. A configurable input stage is routed to one or several of five separate, configurable filtering circuits, and then to a configurable output stage. Amplifier selection and gain, filter corner frequencies, and comparator hysteresis and voltage reference are all easily configurable through the use of jumpers and potentiometers.

Certain types of liquid and gas flow measurement devices utilize a turbine and magnetic sensor to output a sinusoidal signal with a frequency proportional to the rate of flow through the turbine. In order to interface with the Command and Control infrastructure at Kennedy Space Center (KSC), this sinusoidal frequency must be converted into an analog voltage level proportional to the frequency. Existing commercial off-the-shelf (COTS) signal conditioners designed for this task are either obsolete or unqualified for use at KSC. In order to design a replacement signal conditioner that will meet the environmental and operational requirements for use at

KSC, an accurate and reliable analog circuit must be designed to convert the input sine wave into a square wave of the same frequency, while eliminating inaccuracies due to ambient temperature, electromagnetic interference (EMI), and varying signal amplitudes from the turbine sensor. The F2V AFE evaluation board allows side-by-side comparison of several circuit designs to help determine which is optimal.

The F2V AFE evaluation board consists of eight main sections: power, input stage, output stage and five separate, parallel filtering and amplification stages. The power stage accepts external 5 VDC power and generates a –5 VDC supply from this. Both supplies are routed to the other circuit stages. The input stage takes the input sinusoidal signal and passes it through an optional gain amplifier to a header where it can be routed to one or several of the five filter topologies. The output stage contains a header that can be used to select the output of one of the five filters for conversion to a square wave. The five filter topologies represent different methods for amplifying and filtering the input signal. This evaluation board provides a wide array of options for determining the optimal configuration for accurately extracting the

frequency of a sine wave varying in amplitude from 10 mV to >1 V, and in frequency from 20 Hz to 2.5 kHz.

This device is intended to be an evaluation platform for determining an optimum frequency detection circuit design. An evaluation platform benefiting from the constrained routing and component size and placement of surface-mount design, and containing the actual components that will be used in the final design, has many benefits over older breadboard prototyping techniques, where parasitic inductances and capacitance may have a significant effect on test circuits. This device is useful for situations where multiple design options must be compared before a circuit is selected for a final production design. The evaluation board is designed to accurately detect signals from 10 mV peak up to 5 V peak, and frequencies from 20 Hz to 3 kHz, but component substitution will allow both the frequency and voltage range to be significantly expanded or contracted. Other input waveforms, including square waves, can also be processed.

Dust-Tolerant Intelligent Electrical Connection System

This technology has application in aerospace, military, homeland security, mining, and oil and gas exploration operations that are conducted in uncontrolled environments.

John F. Kennedy Space Center, Florida

Faults in wiring systems are a serious concern for the aerospace and aeronautic (commercial, military, and civilian) industries. Circuit failures and vehicle accidents have occurred and have been attributed to faulty wiring created by open and/or short circuits. Often, such circuit failures occur due to vibration during vehicle launch or operation. Therefore, developing non-intrusive fault-tolerant techniques is necessary to

detect circuit faults and automatically route signals through alternate recovery paths while the vehicle or lunar surface systems equipment is in operation. Electrical connector concepts combining dust mitigation strategies and cable diagnostic technologies have significant application for lunar and Martian surface systems, as well as for dusty terrestrial applications.

By creating intelligent electrical con-

nectors that detect, identify, and locate circuit faults and that then bypass damaged conductors and route to available spares, the detection of connector failures is improved, and it becomes possible to recover from mission-threatening circuit faults and failures. Three styles of electrical connector concepts for use in zero-gravity and reduced-gravity dusty environments were developed: conventional connector systems with protective

dust barriers, contactless connector systems, and smooth connector systems. The conventional connector with protective dust barrier mitigates dust by incorporating a physical dust shield. These dust barriers may be retrofitted to existing military or International Space Station connectors. Alternatively, it is possible to utilize existing connectors that can be incorporated into a universal connector housing. Contactless connectors have advantages over conventional connectors where environment integrity poses a design constraint.

The dust-tolerant intelligent electrical connection system has several novel concepts and unique features. It combines intelligent cable diagnostics (health monitoring) and automatic circuit routing capabilities into a dust-tolerant electrical

umbilical. It retrofits a clamshell protective dust cover to an existing connector for reduced gravity operation, and features a universal connector housing with three styles of dust protection: inverted cap, rotating cap, and clamshell. It uses a self-healing membrane as a dust barrier for electrical connectors where required, while also combining lotus leaf technology for applications where a dust-resistant coating providing low surface tension is needed to mitigate Van der Waals forces, thereby disallowing dust particle adhesion to connector surfaces. It also permits using a ruggedized iris mechanism with an embedded electrodynamic dust shield as a dust barrier for electrical connectors where required.

The system also can use a coating to repel lunar dust and self-clean the sur-

face, and incorporates cable health monitoring and automatic routing capabilities into an inductively coupled or capacitively coupled contactless electrical connector. An innovative knob and donut type connector is also included to mitigate lunar dust challenges. Adding electrodynamic dust shields is also possible where needed to combine active dust mitigation with EMI (electromagnetic interference) shielding capability.

Gigabit Ethernet Asynchronous Clock Compensation FIFO

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Clock compensation for Gigabit Ethernet is necessary because the clock recovered from the 1.25 Gb/s serial data stream has the potential to be 200 ppm slower or faster than the system clock. The serial data is converted to 10-bit parallel data at a 125 MHz rate on a clock recovered from the serial data stream. This recovered data needs to be processed by a system clock that is also running at a nominal rate of 125 MHz, but not synchronous to the recovered clock. To cross clock domains, an asynchronous FIFO (first-in-first-out) is used, with the write pointer (wprt) in the recovered clock domain and the read pointer (rptr) in the system clock domain. Because the clocks are generated

from separate sources, there is potential for FIFO overflow or underflow.

Clock compensation in Gigabit Ethernet is possible by taking advantage of the protocol data stream features. There are two distinct data streams that occur in Gigabit Ethernet where identical data is transmitted for a period of time. The first is configuration, which happens during auto-negotiation. The second is idle, which occurs at the end of auto-negotiation and between every packet. The identical data in the FIFO can be repeated by decrementing the read pointer, thus compensating for a FIFO that is draining too fast. The identical data in the FIFO can also be skipped by incrementing the read

pointer, which compensates for a FIFO draining too slowly. The unique and novel features of this FIFO are that it works in both the idle stream and the configuration streams. The increment or decrement of the read pointer is different in the idle and compensation streams to preserve disparity. Another unique feature is that the read pointer to write pointer difference range changes between compensation and idle to minimize FIFO latency during packet transmission.

High-Speed, Multi-Channel Serial ADC LVDS Interface for Xilinx Virtex-5 FPGA

NASA's Jet Propulsion Laboratory, Pasadena, California

Analog-to-digital converters (ADCs) are used in scientific and communications instruments on all spacecraft. As data rates get higher, and as the transition is made from parallel ADC designs to high-speed, serial, low-voltage differential signaling (LVDS) designs, the need will arise to interface these in field-programmable gate arrays (FPGAs). As

Xilinx has released the radiation-hardened version of the Virtex-5, this will likely be used in future missions.

High-speed serial ADCs send data at very high rates. A de-serializer instantiated in the fabric of the FPGA could not keep up with these high data rates. The Virtex-5 contains primitives designed specifically for high-speed, source-syn-

chronous de-serialization, but as supported by Xilinx, can only support bit-widths of 10. Supporting bit-widths of 12 or more requires the use of the primitives in an undocumented configuration, a non-trivial task.

De-serializing the bits from high-speed ADCs running at speeds of 50 Msps or more becomes a non-trivial