dust barriers, contactless connector systems, and smooth connector systems. The conventional connector with protective dust barrier mitigates dust by incorporating a physical dust shield. These dust barriers may be retrofitted to existing military or International Space Station connectors. Alternatively, it is possible to utilize existing connectors that can be incorporated into a universal connector housing. Contactless connectors have advantages over conventional connectors where environment integrity poses a design constraint.

The dust-tolerant intelligent electrical connection system has several novel concepts and unique features. It combines intelligent cable diagnostics (health monitoring) and automatic circuit routing capabilities into a dust-tolerant electrical umbilical. It retrofits a clamshell protective dust cover to an existing connector for reduced gravity operation, and features a universal connector housing with three styles of dust protection: inverted cap, rotating cap, and clamshell. It uses a self-healing membrane as a dust barrier for electrical connectors where required, while also combining lotus leaf technology for applications where a dust-resistant coating providing low surface tension is needed to mitigate Van der Waals forces, thereby disallowing dust particle adhesion to connector surfaces. It also permits using a ruggedized iris mechanism with an embedded electrodynamic dust shield as a dust barrier for electrical connectors where required.

The system also can use a coating to repel lunar dust and self-clean the surface, and incorporates cable health monitoring and automatic routing capabilities into an inductively coupled or capacitively coupled contactless electrical connector. An innovative knob and donut type connector is also included to mitigate lunar dust challenges. Adding electrodynamic dust shields is also possible where needed to combine active dust mitigation with EMI (electromagnetic interference) shielding capability.

This work was done by Mark Lewis, Adam Dokos, Jose Perotti, Carlos Calle, and Robert Mueller of Kennedy Space Center; and Gary Bastin, Jeffrey Carlson, Ivan Townsend III, Christopher Immer, and Pedro Medelius of ASRC Aerospace Corporation. For more information, contact the Kennedy Space Center Innovative Partnerships Office at (321) 867-5033. KSC-13578

Gigabit Ethernet Asynchronous Clock Compensation FIFO

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Clock compensation for Gigabit Ethernet is necessary because the clock recovered from the 1.25 Gb/s serial data stream has the potential to be 200 ppm slower or faster than the system clock. The serial data is converted to 10-bit parallel data at a 125 MHz rate on a clock recovered from the serial data stream. This recovered data needs to be processed by a system clock that is also running at a nominal rate of 125 MHz, but not synchronous to the recovered clock. To cross clock domains, an asynchronous FIFO (first-in-first-out) is used, with the write pointer (wprt) in the recovered clock domain and the read pointer (rptr) in the system clock domain. Because the clocks are generated from separate sources, there is potential for FIFO overflow or underflow.

Clock compensation in Gigabit Ethernet is possible by taking advantage of the protocol data stream features. There are two distinct data streams that occur in Gigabit Ethernet where identical data is transmitted for a period of time. The first is configuration, which happens during auto-negotiation. The second is idle, which occurs at the end of auto-negotiation and between every packet. The identical data in the FIFO can be repeated by decrementing the read pointer, thus compensating for a FIFO that is draining too fast. The identical data in the FIFO can also be skipped by incrementing the read pointer, which compensates for a FIFO draining too slowly. The unique and novel features of this FIFO are that it works in both the idle stream and the configuration streams. The increment or decrement of the read pointer is different in the idle and compensation streams to preserve disparity. Another unique feature is that the read pointer to write pointer difference range changes between compensation and idle to minimize FIFO latency during packet transmission.

This work was done by Jeff Duhachek of Honeywell Aerospace for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809. MSC-24853-1

High-Speed, Multi-Channel Serial ADC LVDS Interface for Xilinx Virtex-5 FPGA

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Analog-to-digital converters (ADCs) are used in scientific and communications instruments on all spacecraft. As data rates get higher, and as the transition is made from parallel ADC designs to high-speed, serial, low-voltage differential signaling (LVDS) designs, the need will arise to interface these in field-programmable gate arrays (FPGAs). As Xilinx has released the radiation-hardened version of the Virtex-5, this will likely be used in future missions.

High-speed serial ADCs send data at very high rates. A de-serializer instantiated in the fabric of the FPGA could not keep up with these high data rates. The Virtex-5 contains primitives designed specifically for high-speed, source-synchronous de-serialization, but as supported by Xilinx, can only support bit-widths of 10. Supporting bit-widths of 12 or more requires the use of the primitives in an undocumented configuration, a non-trivial task.

De-serializing the bits from high-speed ADCs running at speeds of 50 Msps or more becomes a non-trivial

problem in the Xilinx Virtex-5. The bit clock speeds are very high (300 MHz or more), and the ADC sample width can be wider than what the built-in Virtex-5 ISERDES_NODELAY primitives officially support (12 bits or more). The Virtex-5 User Guide does not specify how to configure the ISERDES_NODELAY primitives for such higher bit-widths.

A new SystemVerilog design was written that is simpler and uses fewer hardware resources than the reference design described in Xilinx Application Note XAPP866. It has been shown to work in a Xilinx XC5VSX24OT connected to a MAXIM MAX1438 12-bit ADC using a 50-MHz sample clock. The design can be replicated in the FPGA for multiple ADCs (four instantiations were used for a total of 28 channels).

This work was done by Gregory H. Taylor of Caltech for NASA's Jet Propulsion Laboratory. The software used in this innovation is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. Refer to NPO-48191.