A Robust Strategy for Total Ionizing Dose Testing of Field Programmable Gate Arrays

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ABSTRACT

We present a novel method of FPGA TID testing that measures propagation delay between flip-flops operating at maximum speed. Measurement is performed on-chip at-speed and provides a key design metric when building system-critical synchronous designs.

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I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are widely used in spaceflight applications as controllers and data processors. It has been well-documented that electronics are susceptible to ionizing radiation in the space environment [1,2]. To qualify FPGAs for space operation, the radiation community devoted significant effort to characterizing and understanding their radiation response [3-5].

Traditionally, the scheme for evaluating FPGA total ionizing dose (TID) degradation [4-5] relied on measuring changes in the propagation delay of a specified path after a series of radiation dose steps. Those test paths included an FPGA input, FPGA internal circuitry, an FPGA output, and an external measurement device (*e.g.*, an oscilloscope), as illustrated in Figure 1. At each dose step, the propagation delay is measured from input to output. There are two primary issues with the traditional method:

(1) The propagation path includes a mix of technology, *e.g.*, internal logic and input/output (I/O) logic. In this case, the convolution of degradation information can compromise the device selection process or the device performance integrity during the mission.

(2) Traditional testing methodologies are incapable of capturing sub-nanosecond TID degradation effects with sufficient resolution because measurements are performed external to the device.

The proposed novel technique addresses these two issues. First, as opposed to the traditional method where the delay is measured from input buffer to output buffer, the new method measures a delay from internal element (flip-flop) to internal element. Hence, the data paths under evaluation are purely internal logic and thus avoid convoluted propagation delay contributions. Second, degradation of propagation delay is measured internally for every path in the design. This provides fine granularity and allows for observation of degradation on the order of picoseconds, a substantial improvement on the traditional method.

II. FPGAs & SYNCHRONOUS DESIGN

It is essential for a test methodology to take into account all the elements that make up the device under test (DUT). This includes the basic building blocks contained in the FPGA and the topology of block connections used in the design. The following sections correlate the proposed TID test methodology to FPGA structures and common design practice for critical missions.

A. FPGA Structure

There are three primary categories of structures that exist in an FPGA: configuration, functional logic data path, and global routing. Each category has a unique contribution to the overall radiation tolerance of a design. The configuration is a set of switches that defines the state of functional data path and global route elements for a particular design. An FPGA design is implemented by selecting a switch state – on or off – to build logic and connectivity. As an example, a Microsemi ProASIC3 FPGA [7] logic block is illustrated in Figure 2. The figure shows how switches are set to define the logic block's function in a design. The ProASIC3 FPGA uses flash-type configuration memory cells to control the state of the switches shown throughout Figure 2. Accumulated charge in these floating-gate flash cells will increase the delay of its switch and hence erode performance of each FPGA element [7]. In fact, different configurations will utilize different numbers of floating-gate cells in each logic block, allowing for the possibility of design-dependent radiation responses.

B. Topology of Critical Designs and Synchronous Methodology

The most common design topology now used for critical missions is synchronous design [6]. Therefore, test structures used to characterize TID effects in designs targeted for critical applications should also adhere to the synchronous design methodology. Basic building blocks in a synchronous FPGA design include: combinatorial logic, D flip-flops (DFF), local routes, global routes (clocks and resets), and I/O. The design topology is defined by how these elements are utilized and connected to create a specified function.

A synchronous design is a compute-and-sample system made up of data paths. An internal data path is defined as the logic contained in-route from flip-flop to flip-flop, *i.e.*, a Start-Point DFF to an End-Point DFF. Each End-Point DFF can have several data paths that feed its input pin, called fan-in. Each End-Point DFF's input pin is sampled at every clock edge. The End-Point DFF and its incoming data paths

are referred to as a cone-of-logic. Figure 3 illustrates two separate cones-of-logic: one cone-of-logic with an End-Point DFF that has several input data paths (fan-in > 1), and another cone-of-logic with one input path (fan-in = 1).

C. Data Path Propagation Delays in Synchronous Designs

Every data path in a synchronous design has a unique delay (τ_{dly}), as shown in Figure 3. τ_{dly} is defined as the time it takes for a signal to launch from a Start-Point and propagate to its End-Point. A strict definition and requirement of synchronous methodology is that for all data paths in the design, τ_{dly} must not exceed the clock period (τ_{clk}). If this requirement is violated, the design will contain data paths that behave unreliably and in most cases will be inoperable [6]. This timing requirement is the foundation of the proposed TID test methodology.

III. New Test Methodology

A. New Test Procedure

The novel approach uses synchronous designs as test structures and focuses on τ_{dly}. As a reminder, τ_{dly} is the propagation delay from one DFF to the next DFF and is illustrated in Figure 3. The test structures are operated such that their maximum delay path is approximately equal to the clock period (i.e., τ_{dly} τ_{clk}). This stresses the DUT in such a way that any degradation in τ_{dly} will violate data-path timing and make the design inoperable at the current clock frequency under test.

The testing procedure is as follows: First, experimentally determine the minimum clock period, *i.e.*, maximum clock frequency, of each test structure. This is done by fine-tuning the operational frequency to observe at which frequency the test structure is functional versus when it is not. This is an indirect measurement of each test structure's maximum path delay because τ_{dly} τ_{clk}. Clock period tuning should be on the order of picoseconds. Second, irradiate the DUT. Third, experimentally determine the new post-irradiation minimum clock period. This is a measurement of each test structure's current maximum path delay. The difference between the current and pre-irradiation clock periods measures degradation in τ_{dly} between DFFs, which we define as the key metric for TID degradation.

B. Key Advantages

We define failure in equivalent terms a designer can use directly, which is a key advantage of our method. For a synchronous circuit, failure will occur when $\tau_{dly} > \tau_{clk}$. Many designs require a 10% design margin from the estimated maximum clock speed, which is calculated using Static Timing Analysis (STA) tools. Testing τ_{dly} until that 10% line is crossed is a clear, application-driven failure point, as opposed to referencing a 10% decrease in input-to-output propagation delay. Arbitrarily-chosen failure mechanisms are less useful for a designer, who must figure out what parameters are quantified by that 10% change and how they may affect each design. It is preferable to use τ_{dly} degradation measurements because they can directly correlate TID data with the terminology and tools used by designers who may not have a radiation background. The increased delay can be accounted for in a design, along with typical margins, to create a robust design capable of operating at predicted total dose levels.

Another key advantage is that τ_{dly} can be quantified with much finer resolution than with previous test methods. When measuring propagation delay externally (as in Figure 1), the measurement is often in hundreds of nanoseconds [4] due to the sheer amount of internal circuitry measured and equipment limitations. Any small change in performance is lost in the noise and jitter levels and cannot be directly attributable to a particular component of the FPGA. However, by using data-path DFFs as the test points (*c.f.*, Figure 4), changes on the order of picoseconds are observable.

IV. Experimental Results

A. Degradation from Pre-Rad Data

We designed and implemented a set of test structures in Microsemi ProASIC3 flash-based FPGAs to evaluate the feasibility of our new TID test methodology. The test structures are described in Table I, and include four different windowed shift registers (WSRs) with varying lengths of intermediate logic

between DFFs. Additionally, a set of counter arrays was designed to evaluate the effects of increased circuit complexity on degradation.

The test structures were exposed to 45 krad(Si) of total dose from gamma irradiation at a dose rate of 1 rad(Si)/s. At 25 krad(Si), the worst-performing part showed a 10% τ_{dly} degradation. After approximately 35 krad(Si), all parts showed a sharp increase in τ_{dly} beyond 10%. Figure 5 shows the gradual increase in minimum clock period (τ_{clk}), which correlates to increased τ_{dly} in the data-paths. The more complex counter arrays showed a faster degradation, with both parts reaching 10% degradation at or just beyond 20 krad(Si).

B. Real-World Design Impact and Analysis

TID degradation is usually reported as a percentage change from pre-radiation values [4-5]. However, the percentage of measured degradation should not be applied to a design if the degradation metric during testing does not correspond to the definition of degradation in the real world design topology. As previously discussed, that metric of degradation is $\tau_{dly.}$ τ_{dly} is also the metric used in STA to determine the operability timing constraints of a synchronous design. Therefore, when using τ_{dly} as the degradation metric, the designer can take the results and incorporate them into the design flow.

Figure 6 shows the degradation in clock period for the counter arrays as compared to the STA estimates. Those estimates are conservative, so note that a designer who implements a realistic 10% derating beyond the STA estimate will not actually see failure ($\tau_{dly} > \tau_{clk}$) until a higher total dose of 35 krad(Si). Furthermore, the increased radiation response of the more complex counter arrays reinforces that it is important to vary test structure complexity in order to develop radiation response trends. Fortunately, the new test method lends itself to testing such complex test structures because degradation is measured in the high-speed internal logic, rather than at the output, so it can be finely measured with picosecond precision.

V. SUMMARY

Our test procedure provides a more robust, more precise, and more design-applicable set of radiation data for designers than previous test methods, especially when working with synchronous designs. It provides a means of capturing τ_{dly} degradation on-chip and at-speed, rather than relying on external test setups. The τ_{dly} data are then directly portable to any synchronous design, so that an engineer building a critical system may model how a predicted level of total ionizing dose will affect the timing of that system. With that knowledge, the designer can then incorporate sufficient timing margins to allow safe, reliable operation of the critical system. The final paper will include more information on annealing, and the relationship between complexity and degradation will be further explored.

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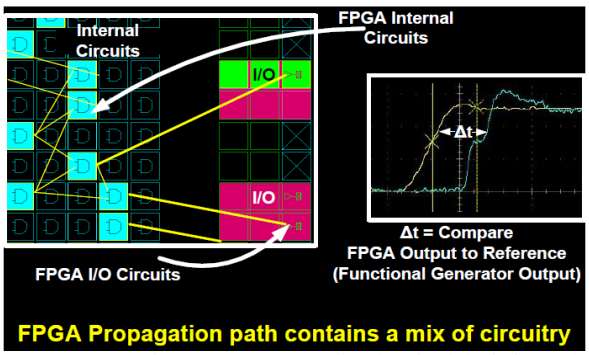

Figure 1. External measurement setup showing that it includes a mix of device technologies in one measurement.

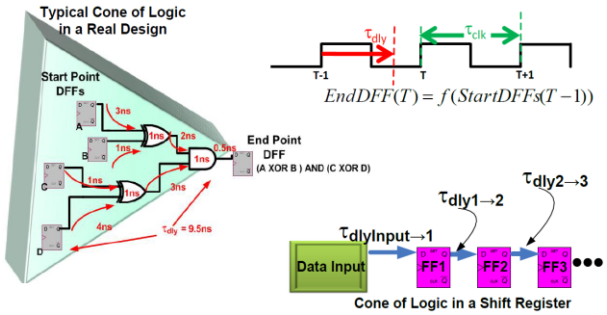

Figure 3. Diagram of synchronous design cone-of-logic and corresponding timing delays.

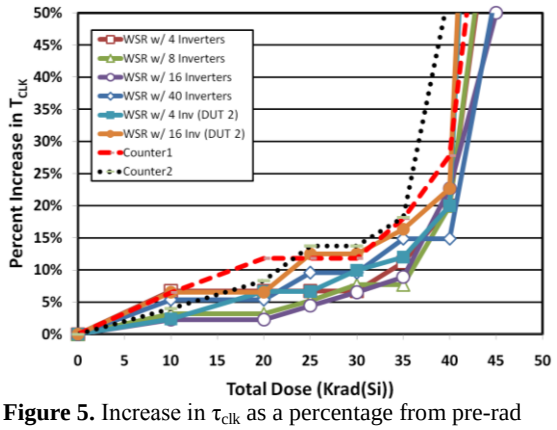

Figure 5. Increase in τ_{clk} as a percentage from pre-rad levels for WSRs (solid) and counters (dotted).

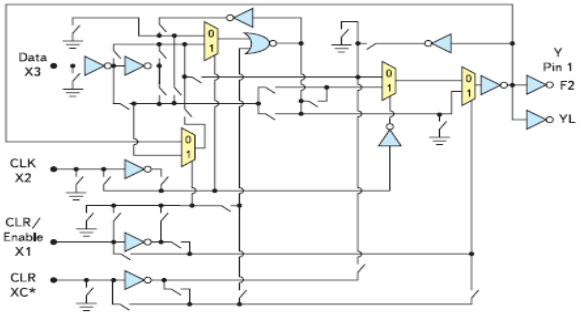

Figure 2. One functional building block in the Microsemi ProASIC3 FPGA, capable of forming any standard logic gate or flip flop. Note the large number of flash-based switches in any signal path.

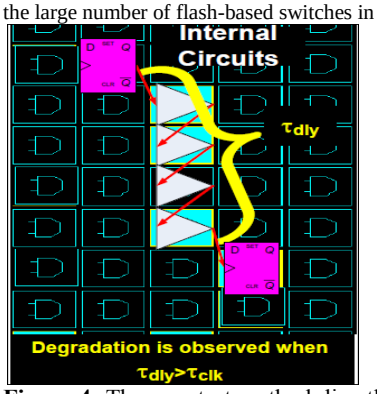

Figure 4. The new test method directly measures delay from one DFF to the next, with no external signals.

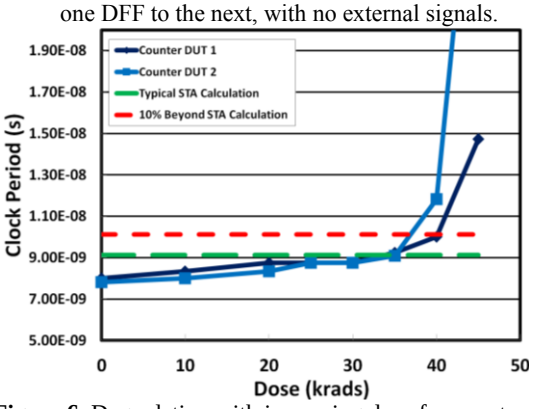

Figure 6. Degradation with increasing dose for counter circuits, plotted with Static Timing Analysis estimates.

TABLE I
TEST STRUCTURES

ID	# of DFFs	Inverter stages	Predicted Speed (MHz) Best/Typ/Worst	Actual Speed DUT1/DUT2 (MHz)	Best Measurement Resolution[1] (ps)
A	100	40	56.3/46.1/41.5	54.2/52.0	202
B	800	4	299/299/280	325/313	42
C	800	8	231/189/170	194/194	103
D	800	16	131/107/96	110/110	184
Counters	NA	NA	133/109/98	125/128	142

[1]Measurement resolution was limited only by the onboard clock generators in the custom tester. By supplying a high-quality external clock signal, measurement resolution can be as low as desired. For example, by adjusting clock frequency from 300 MHz to 300.1 MHz, a ~1ps granularity is possible.