

The FPGA implementation offers a low-cost, flexible solution compared to traditional ASIC (application specific integrated circuit) and can be integrated as an intellectual property (IP) for part of, e.g., a design that manages the instrument interface. The FPGA implementation was benchmarked on the Xilinx Virtex IV LX25 device, and ported to a Xilinx prototype board. The

current implementation has a critical path of 29.5 ns, which dictated a clock speed of 33 MHz. The critical path delay is end-to-end measurement between the uncompressed input data and the output compression data stream. The implementation compresses one sample every clock cycle, which results in a speed of 33 Msample/s. The implementation has a rather low device use of the

Xilinx Virtex IV LX25, making the total power consumption of the implementation about 1.27 W.

This work was done by Didier Keymeulen, Nazeeh I. Aranki, and Matthew A. Klimesh of Caltech, and Alireza Bakhshi of B&A Engineering for NASA's Jet Propulsion Laboratory. For more information, contact iaofjice@jpl.nasa.gov. NPO-47103

High-Voltage, Low-Power BNC Feedthrough Terminator

John F. Kennedy Space Center, Florida

This innovation is a high-voltage, low-power BNC (Bayonet Neill–Concelman) feedthrough that enables the user to terminate an instrumentation cable properly while connected to a high voltage, without the use of a voltage divider. This feedthrough is low power, which will not load the source, and will properly terminate the instrumentation cable to the instrumentation, even if the cable impedance is not constant.

The Space Shuttle Program had a requirement to measure voltage transients on the orbiter bus through the Ground Lightning Measurement System (GLMS). This measurement has a bandwidth requirement of 1 MHz. The GLMS voltage measurement is connected to the or-

biter through a DC panel. The DC panel is connected to the bus through a non-uniform cable that is approximately 75 ft (≈ 23 m) long. A 15-ft (≈ 5 -m), 50-ohm triaxial cable is connected between the DC panel and the digitizer. Based on calculations and simulations, cable resonances and reflections due to mismatched impedances of the cable connecting the orbiter bus and the digitizer causes the output not to reflect accurately what is on the bus. A voltage divider at the DC panel, and terminating the 50-ohm cable properly, would eliminate this issue. Due to implementation issues, an alternative design was needed to terminate the cable properly without the use of a voltage divider.

Analysis shows how the cable resonances and reflections due to the mismatched impedances of the cable connecting the orbiter bus and the digitizer causes the output not to reflect accurately what is on the bus. After simulating a dampening circuit located at the digitizer, simulations were performed to show how the cable resonances were dampened and the accuracy was improved significantly. Test cables built to verify simulations were accurate. Since the dampening circuit is low power, it can be packaged in a BNC feedthrough.

This work was done by Douglas (Doug) Bearden of Kennedy Space Center. Further information is contained in a TSP (see page 1). KSC-13560

SpaceCube Mini

A unit that is being designed will be a very compact and low-power system.

Goddard Space Flight Center, Greenbelt, Maryland

This version of the SpaceCube will be a full-fledged, onboard space processing system capable of 2500+ MIPS, and featuring a number of plug-and-play gigabit and standard interfaces, all in a condensed 3×3×3 form factor [<10 watts and < 3 lb (≈ 1.4 kg)]. The main processing engine is the Xilinx SIRF radiation-hardened-by-design Virtex-5 FX-130T field-programmable gate array (FPGA).

Even as the SpaceCube 2.0 version (currently under test) is being targeted as the platform of choice for a number of the upcoming Earth Science Decadal Survey missions, GSFC has been contacted by customers who wish to see a system that incorporates key features of the version 2.0 architecture in an even smaller form factor. In order to fulfill

that need, the SpaceCube Mini is being designed, and will be a very compact and low-power system. A similar flight system with this combination of small size, low power, low cost, adaptability, and extremely high processing power does not otherwise exist, and the SpaceCube Mini will be of tremendous benefit to GSFC and its partners.

The SpaceCube Mini will utilize space-grade components. The primary processing engine of the Mini is the Xilinx Virtex-5 SIRF FX-130T radiation-hardened-by-design FPGA for critical flight applications in high-radiation environments. The Mini can also be equipped with a commercial Xilinx Virtex-5 FPGA with integrated PowerPCs for a low-cost, high-power computing platform for use in the relatively radia-

tion-benign LEOs (low-Earth orbits). In either case, this version of the SpaceCube will weigh less than 3 pounds (≈ 1.4 kg), conform to the CubeSat form-factor (10×10×10 cm), and will be low power (<10 watts for typical applications). The SpaceCube Mini will have a radiation-hardened Aeroflex FPGA for configuring and scrubbing the Xilinx FPGA by utilizing the onboard FLASH memory to store the configuration files. The FLASH memory will also be used for storing algorithm and application code for the PowerPCs and the Xilinx FPGA. In addition, it will feature high-speed DDR SDRAM (double data rate synchronous dynamic random-access memory) to store the instructions and data of active applications. This version will also feature SATA-II and Gigabit

Ethernet interfaces. Furthermore, there will also be general-purpose, multi-gigabit interfaces. In addition, the system will have dozens of transceivers that can support LVDS (low-voltage differential signaling), RS-422, or SpaceWire. The SpaceCube Mini includes an I/O card that can be customized to meet the needs of each mission. This version of the SpaceCube will be designed so that multiple Minis can be networked to-

gether using SpaceWire, Ethernet, or even a custom protocol.

Scalability can be provided by networking multiple SpaceCube Minis together. Rigid-Flex technology is being targeted for the construction of the SpaceCube Mini, which will make the extremely compact and low-weight design feasible. The SpaceCube Mini is designed to fit in the compact CubeSat form factor, thus allowing deployment in

a new class of missions that the previous SpaceCube versions were not suited for. At the time of this reporting, engineering units should be available in the summer 2012.

This work was done by Michael Lin, David Petrick, Alessandro Geist, and Thomas Flatley of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16223-1

Dichroic Filter for Separating W-Band and Ka-Band

NASA's Jet Propulsion Laboratory, Pasadena, California

The proposed Aerosol/Cloud/Ecosystems (ACEs) mission development would advance cloud profiling radar from that used in CloudSat by adding a 35-GHz (Ka-band) channel to the 94-GHz (W-band) channel used in CloudSat. In order to illuminate a single antenna, and use CloudSat-like quasi-optical transmission lines, a spatial diplexer is needed to add the Ka-band channel.

A dichroic filter separates Ka-band from W-band by employing advances in electrical discharge machining (EDM) and mode-matching analysis techniques developed and validated for designing dichroics for the Deep Space Network (DSN), to develop a preliminary design that both met the requirements of frequency separation and mechanical strength.

First, a mechanical prototype was built using an approximately 102-micron-diameter EDM process, and tolerances of the hole dimensions, wall thickness, radius, and dichroic filter thickness measured. The prototype validated the manufacturing needed to design a dichroic filter for a higher-frequency usage than previously used in the DSN. The initial design was based on a Ka-band design, but thicker walls are required for mechanical rigidity than one obtains by simply scaling the Ka-band dichroic filter. The resulting trade of hole dimensions for mechanical rigidity (wall thickness) required electrical redesign of the hole dimensions. Updates to existing codes in the linear solver decreased the analysis time using mode-matching, en-

abling the electrical design to be realized quickly.

This work is applicable to missions and instruments that seek to extend W-band cloud profiling measurements to other frequencies. By demonstrating a dichroic filter that passes W-band, but reflects a lower frequency, this opens up the development of instruments that both compare to and enhance CloudSat.

This work was done by Larry W. Epp, Stephen L. Durden, Vahraz Jamnejad, Ezra M. Long, John B. Sosnowski, Raymond J. Higuera, and Jacqueline C. Chen of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-48174