Compact Receiver Front Ends for Submillimeter-Wave Applications

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The current generation of submillimeter-wave instruments is relatively mass- and power-hungry. The receiver front ends (RFEs) of a submillimeter instrument form the heart of the instrument, and any mass reduction achieved in this subsystem is propagated through the instrument. In the current implementation, the RFE consists of different blocks for the mixer and LO circuits. The motivation for this work is to reduce the mass of the RFE by integrating the mixer and LO circuits in one waveguide block.

The mixer and its associated LO chips will all be packaged in a single waveguide package. This will reduce the mass of the RFE and also provide a number of other advantages. By bringing the mixer and LO circuits close together, losses in the waveguide will be reduced. Moreover, the compact nature of the block will allow for better thermal control of the block, which is important in order to reduce gain fluctuations.

A single waveguide block with a 600-GHz RFE functionality (based on a sub-harmonically pumped Schottky diode pair) has been demonstrated. The block is about 3×3×3 cm^3. The block combines the mixer and multiplier chip in a single package. 3D electromagnetic simulations were carried out to design the waveguide circuit around the mixer and multiplier chip. The circuit is optimized to provide maximum output power and maximum bandwidth.

An integrated submillimeter front end featuring a 520–600-GHz sub-harmonic mixer and a 260–300-GHz frequency tripler in a single cavity was tested. Both devices used GaAs MMIC membrane planar Schottky diode technology. The sub-harmonic mixer/tripler circuit has been tested using conventional metal-machined blocks. Measurement results on the metal block give best DSB (double sideband) mixer noise temperature of 2,360 K and conversion losses of 7.7 dB at 520 GHz. The LO input power required to pump the integrated tripler/sub-harmonic mixer is between 30 and 50 mW.

This work was done by Imran Mehdi, Goutam Chattopadhyay, Erich T. Schlecht, Robert H. Lin, Seth Sin, Alejandro Peralta, Choonsup Lee, John J. Gill, Samuel Gulkis, and Bertrand C. Thomas of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-47902

Dynamically Reconfigurable Systolic Array Accelerator

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A polymorphic systolic array framework has been developed that works in conjunction with an embedded microprocessor on a field-programmable gate array (FPGA), which allows for dynamic and complimentary scaling of acceleration levels of two algorithms active concurrently on the FPGA. Use is made of systolic arrays and a hardware-software co-design to obtain an efficient multi-application acceleration system. The flexible and simple framework allows hosting of a broader range of algorithms, and is extendable to more complex applications in the area of aerospace embedded systems.

FPGA chips can be responsive to real-time demands for changing applications' needs, but only if the electronic fabric can respond fast enough. This systolic array framework allows for rapid partial and dynamic reconfiguration of the chip in response to the real-time needs of scalability, and adaptability of executables.

This work was done by Aravind Dasu and Robert Barnes of Utah State University Research for Goddard Space Flight Center. For further information, contact the Goddard Innovative Partnerships Office at (301) 286-5810. GSC-16303-1

Blocking Losses With a Photon Counter

Losses for single detectors and arrays of detectors are characterized.

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It was not known how to assess accurately losses in a communications link due to photodetector blocking, a phenomenon wherein a detector is rendered inactive for a short time after the detection of a photon. When used to detect a communications signal, blocking leads to losses relative to an ideal detector, which may be measured as a reduction in the communications rate for a given received signal power, or an increase in the signal power required to support the same communications rate. This work involved characterizing blocking losses for single detectors and arrays of detectors.

Blocking may be mitigated by spreading the signal intensity over an array of detectors, reducing the count rate on any one detector. A simple approximation was made to the blocking loss as a