# Single-Pole Double-Throw MMIC Switches for a Microwave Radiometer

**Switches reduce the effect of gain and noise instabilities.**

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In order to reduce the effect of gain and noise instabilities in the RF chain of a microwave radiometer, a Dicke radiometer topology is often used, as in the case of the proposed surface water and ocean topography (SWOT) radiometer instrument. For this topology, a single-pole double-throw (SPDT) microwave switch is needed, which must have low insertion loss at the radiometer channel frequencies to minimize the overall receiver noise figure. Total power radiometers are limited in accuracy due to the continuous variation in gain of the receiver. Currently, there are no switches in the market that can provide these characteristics at 92, 130, and 166 GHz as needed for the proposed SWOT radiometer instrument.

High-frequency SPDT switches were developed in the form of monolithic microwave integrated circuits (MMICs) using 75-μm indium phosphide (InP) PIN-diode technology. These switches can be easily integrated into Dicke switched radiometers that utilize microstrip technology. The MMIC switches operate from 80 to 105 GHz, 90 to 135 GHz, and 160 to 185 GHz. The 80- to 105-GHz switches have been tested and have achieved <2-dB insertion loss, >15-dB return loss (>18 dB for the asymmetric design), and >15-dB isolation. The isolation can be tuned to achieve >20-dB isolation from 85 to 103 GHz. The 90- to 135-GHz SPDT switch has achieved <2-dB insertion loss, >15-dB return loss, and 8- to 12-dB isolation. However, it has been shown that the isolation of this switch can also be improved. Although the 160- to 185-GHz switch has been fabricated, it has not yet been measured at the time of this reporting. Simulation results predict this switch will have <2-dB insertion loss, >20-dB return loss, and >20-dB isolation.

The switches can be used for a radiometer such as the one proposed for the SWOT Satellite Mission whose three channels at 92, 130, and 166 GHz would allow for wet-tropospheric path delay correction near coastal zones and over land. This feat is not possible with the current Jason-class radiometers due to their lower frequency signal measurement and thus lower resolution.

*The design work was done by Oliver Montes, Douglas E. Dawson, and Pekka P. Kangaslahti of Caltech for NASA's Jet Propulsion Laboratory. The processing of the InP MMIC circuits was done by Kwok Loi and Augusto Gutierrez from NGST. Further information is contained in a TSP (see page 1).* NPO-48083

# On Shaft Data Acquisition System (OSDAS)

**Applications include helicopter rotor testing, onboard liquid/solid rocket engine data acquisition, and gas-turbine-engine health monitoring.**

*Marshall Space Flight Center, Alabama*

On Shaft Data Acquisition System (OSDAS) is a rugged, compact, multiple-channel data acquisition computer system that is designed to record data from instrumentation while operating under extreme rotational centrifugal or gravitational acceleration forces. This system, which was developed for the Heritage Fuel Air Turbine Test (HFATT) program, addresses the problem of recording multiple channels of high-sample-rate data on most any rotating test article by mounting the entire acquisition computer onboard with the turbine test article. With the limited availability of slip ring wires for power and communication, OSDAS utilizes its own resources to provide independent power and amplification for each instrument. Since OSDAS utilizes standard PC technology as well as shared code interfaces with the next-generation, real-time health monitoring system (SPARTAA — Scalable Parallel Architecture for Real Time Analysis and Acquisition), this system could be expanded beyond its current capabilities, such as providing advanced health monitoring capabilities for the test article.

High-conductor-count slip rings are expensive to purchase and maintain, yet only provide a limited number of conductors for routing instrumentation off the article and to a stationary data acquisition system. In addition to being limited to a small number of instruments, slip rings are prone to wear quickly, and introduce noise and other undesirable characteristics to the signal data. This led to the development of a system capable of recording high-density instrumentation, at high sample rates, on the test article itself, all while under extreme rotational stress.

OSDAS is a fully functional PC-based system with 48 channels of 24-bit, high-sample-rate input channels, phase synchronized, with an onboard storage capacity of over ½-terabyte of solid-state storage. This recording system takes a novel approach to the problem of recording multiple channels of instrumentation, integrated with the test article itself, packaged in a compact/rugged form factor, consuming limited power, all while rotating at high turbine speeds.

The hardware components were oriented, secured, and encapsulated by a variety of novel application techniques that allow for the system to continue operation under rotational stress. This full, custom-hardened system was designed to be a comprehensive solution to attaching directly to instrumentation (without external sensor power supplies and amplification). Instead, all instrumentation has a dedicated power supply, integrated inside OSDAS, with the ability to withstand electrical faults (short circuits, etc.) without compromising other sensors. The amplification required for each sensor was configurable at build time to match that of the Kulite instrumentation used in the HFATT article. The entire computing, storage, and acquisition hardware system was custom-encapsulated in a thermally conductive medium that allows heat to passively dissipate by air via the outer shell (indoor/out-

door environmental conditions) or by conduction cooling in space conditions.

OSDAS is a comprehensive, high-capacity acquisition system capable of withstanding extreme rotational forces. The existing products on the market are either limited in channel capacity, bandwidth, or simply not capable of withstanding physical stress. As part of the build process, a variety of mounting and encapsulation techniques was utilized, which ensures the system can withstand harsh rotational stresses. OSDAS employs the use of standard PC technology. The system was built to share a code interface with that of the SPARTAA, otherwise known as the next-generation, real-time vibration monitoring system (RTVMS). This allows OSDAS to be expanded in the future to incorporate real-time health monitoring of the test article hardware.

OSDAS employs a common hardware-mounting interface that allows the acquisition system to be adapted to a variety of test articles and environments. With the use of built-in sensor amplification and independent power supplies, a total sensor acquisition solution was provided. While acquisition storage capacity and channel counts were limited initially by the desire of a small/compact form factor, further expansion beyond 48 channels and multi-terabyte solutions is possible. For the final system checkout, OSDAS was subjected to speeds over 15,000 RPM (maximum facility capability). A continuous Ethernet connection was maintained throughout the checkout and test series.

*This work was done by Marc Pedings, Shawn DeHart, Jason Formby, and Charles Naumann of Optical Sciences Corporation for Marshall Space Flight Center. For more information, contact Sammy Nabors, MSFC Commercialization Assistance Lead, at sammy.a.nabors@nasa.gov. Refer to MFS-32908-1.*

# ASIC Readout Circuit Architecture for Large Geiger Photodiode Arrays

## Commercial applications include 3D imaging, positron emission tomography (PET), laser ranging (LADAR), night vision, and surveillance.

*Goddard Space Flight Center, Greenbelt, Maryland*

The objective of this work was to develop a new class of readout integrated circuit (ROIC) arrays to be operated with Geiger avalanche photodiode (GPD) arrays, by integrating multiple functions at the pixel level (smart-pixel or active pixel technology) in 250-nm CMOS (complementary metal oxide semiconductor) processes. In order to pack a maximum of functions within a minimum pixel size, the ROIC array is a full, custom application-specific integrated circuit (ASIC) design using a mixed-signal CMOS process with compact primitive layout cells.

The ROIC array was processed to allow assembly in bump-bonding technology with photon-counting infrared detector arrays into 3-D imaging cameras (LADAR). The ROIC architecture was designed to work with either common-anode Si GPD arrays or common-cathode InGaAs GPD arrays. The current ROIC pixel design is hardwired prior to processing one of the two GPD array configurations, and it has the provision to allow soft reconfiguration to either array (to be implemented into the next ROIC array generation). The ROIC pixel architecture implements the Geiger avalanche quenching, bias, reset, and time to digital conversion (TDC) functions in full-digital design, and uses time domain over-sampling (vernier) to allow high temporal resolution at low clock rates, increased data yield, and improved utilization of the laser beam.

The non-uniformity of the breakdown voltage over large GPD arrays (a serious concern in InGaAs GPD arrays) is partially corrected by a digital-to-analog circuit, capable of detecting the first breakdown event at pixel level, storing the breakdown voltage bin, and correcting for the breakdown voltage excursion. The correction is written at the pixel level. It is performed once at the first power-up and could be repeated any time prior to field operation after ROIC hard reset. Implementing this feature is critical for large and very large GPD arrays, for which I/O limitations impose on-die time binning on multiple pixels.

A pixel-level interface integrated into the ROIC pixel was developed to work with the GPD pixel (active quenching or AQC). The AQC interface detects the Geiger pulse, quenches the Geiger avalanche, and then resets (drains) the charge at the GPD-AQC node. The ROIC-GPD array is fully gated — GATE enable generates the START signal for the pixel-level TDCs and biases the GPD pixel above the breakdown voltage. The stop event in TDC is driven by the AQC output (following the photon detection registration) and identifies the time stamp with respect to the system clock generating the synchronized GATE (START) signal. The signal is fed through multiple taps for fine time sampling (vernier bits) to a synchronized random counter. A programmable delay in the time vernier module allows extending the dynamic range without adding counter bits to the raw range TDC module, but at the expense of decreased timing resolution. ROIC arrays processed in 250-nm CMOS allowed increasing the count rate of the Geiger arrays (less than 20-ns reset) and reading out the time stamp of Geiger events detected in each pixel with 350-ps timing resolution. Fine time sampling is created by using redundant clock phase shifting as a time vernier, thus allowing the pixel to over-sample the time domain at low clock frequency (200 MHz), and thus decreasing the uncertainty due to setup time violations and improving the utilization of the laser pulses. The programmable delay allows also super-fine timing — in this mode the ROIC should be capable of 175-ps timing resolution. The row-column driver, integrated with the ROIC array, enables shifting sequentially the row data. The implementation into 16×32 or mosaic 32×32 pixel ROIC arrays should be scalable to much larger ROIC/GPD arrays.

*This work was done by Stefan Vasile and Jerold Lipson of aPeak Inc. for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16107-1*