door environmental conditions) or by conduction cooling in space conditions.

OSDAS is a comprehensive, high-capacity acquisition system capable of withstanding extreme rotational forces. The existing products on the market are either limited in channel capacity, bandwidth, or simply not capable of withstanding physical stress. As part of the build process, a variety of mounting and encapsulation techniques was utilized, which ensures the system can withstand harsh rotational stresses. OSDAS employs the use of standard PC technology. The system was built to share a code interface with that of the SPARTAA, otherwise known as the next-generation, real-time vibration monitoring system (RTVMS). This allows OSDAS to be expanded in the future to incorporate real-time health monitoring of the test article hardware.

OSDAS employs a common hardware-mounting interface that allows the acquisition system to be adapted to a variety of test articles and environments. With the use of built-in sensor amplification and independent power supplies, a total sensor acquisition solution was provided. While acquisition storage capacity and channel counts were limited initially by the desire of a small/compact form factor, further expansion beyond 48 channels and multi-terabyte solutions is possible. For the final system checkout, OSDAS was subjected to speeds over 15,000 RPM (maximum facility capability). A continuous Ethernet connection was maintained throughout the checkout and test series.

# ASIC Readout Circuit Architecture for Large Geiger Photodiode Arrays

## Commercial applications include 3D imaging, positron emission tomography (PET), laser ranging (LADAR), night vision, and surveillance.

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The objective of this work was to develop a new class of readout integrated circuit (ROIC) arrays to be operated with Geiger avalanche photodiode (GPD) arrays, by integrating multiple functions at the pixel level (smart-pixel or active pixel technology) in 250-nm CMOS (complementary metal oxide semiconductor) processes. In order to pack a maximum of functions within a minimum pixel size, the ROIC array is a full, custom application-specific integrated circuit (ASIC) design using a mixed-signal CMOS process with compact primitive layout cells.

The ROIC array was processed to allow assembly in bump-bonding technology with photon-counting infrared detector arrays into 3-D imaging cameras (LADAR). The ROIC architecture was designed to work with either common-anode Si GPD arrays or common-cathode InGaAs GPD arrays. The current ROIC pixel design is hardwired prior to processing one of the two GPD array configurations, and it has the provision to allow soft reconfiguration to either array (to be implemented into the next ROIC array generation). The ROIC pixel architecture implements the Geiger avalanche quenching, bias, reset, and time to digital conversion (TDC) functions in full-digital design, and uses time domain over-sampling (vernier) to allow high temporal resolution at low clock rates, increased data yield, and improved utilization of the laser beam.

The non-uniformity of the breakdown voltage over large GPD arrays (a serious concern in InGaAs GPD arrays) is partially corrected by a digital-to-analog circuit, capable of detecting the first breakdown event at pixel level, storing the breakdown voltage bin, and correcting for the breakdown voltage excursion. The correction is written at the pixel level. It is performed once at the first power-up and could be repeated any time prior to field operation after ROIC hard reset. Implementing this feature is critical for large and very large GPD arrays, for which I/O limitations impose on-die time binning on multiple pixels.

A pixel-level interface integrated into the ROIC pixel was developed to work with the GPD pixel (active quenching or AQC). The AQC interface detects the Geiger pulse, quenches the Geiger avalanche, and then resets (drains) the charge at the GPD-AQC node. The ROIC-GPD array is fully gated — GATE enable generates the START signal for the pixel-level TDCs and biases the GPD pixel above the breakdown voltage. The stop event in TDC is driven by the AQC output (following the photon detection registration) and identifies the time stamp with respect to the system clock generating the synchronized GATE (START) signal. The signal is fed through multiple taps for fine time sampling (vernier bits) to a synchronized random counter. A programmable delay in the time vernier module allows extending the dynamic range without adding counter bits to the raw range TDC module, but at the expense of decreased timing resolution. ROIC arrays processed in 250-nm CMOS allowed increasing the count rate of the Geiger arrays (less than 20-ns reset) and reading out the time stamp of Geiger events detected in each pixel with 350-ps timing resolution. Fine time sampling is created by using redundant clock phase shifting as a time vernier, thus allowing the pixel to over-sample the time domain at low clock frequency (200 MHz), and thus decreasing the uncertainty due to setup time violations and improving the utilization of the laser pulses. The programmable delay allows also super-fine timing — in this mode the ROIC should be capable of 175-ps timing resolution. The row-column driver, integrated with the ROIC array, enables shifting sequentially the row data. The implementation into 16×32 or mosaic 32×32 pixel ROIC arrays should be scalable to much larger ROIC/GPD arrays.