Books & Reports

⚙ Mars Technology Rover with Arm-Mounted Percussive Coring Tool, Microimager, and Sample-Handling Encapsulation Containerization Subsystem

A report describes the PLuto (programmable logic) Mars Technology Rover, a mid-sized FIDO (field integrated design and operations) class rover with six fully drivable and steerable cleated wheels, a rocker-bogey suspension, a pan-tilt mast with panorama and navigation stereo camera pairs, forward and rear stereo hazcam pairs, internal avionics with motor drivers and CPU, and a 5-degrees-of-freedom robotic arm.

The technology rover was integrated with an arm-mounted percussive coring tool, microimager, and sample handling encapsulation containerization subsystem (SHEC). The turret of the arm contains a percussive coring drill and microimager. The SHEC sample caching system mounted to the rover body contains coring bits, sample tubes, and sample plugs.

The coring activities performed in the field provide valuable data on drilling conditions for NASA tasks developing and studying coring technology. Caching of samples using the SHEC system provide insight to NASA tasks investigating techniques to store core samples in the future.

This work was done by Paulo J. Younse, Matthew A. Dicicco, and Albert R. Morgan of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47917

☄ Fault-Tolerant, Real-Time, Multi-Core Computer System

A document discusses a fault-tolerant, self-aware, low-power, multi-core computer for space missions with thousands of simple cores, achieving speed through concurrency. The proposed machine decides how to achieve concurrency in real time, rather than depending on programmers. The driving features of the system are simple hardware that is modular in the extreme, with no shared memory, and software with significant run-time reorganizing capability.

The document describes a mechanism for moving ongoing computations and data that is based on a functional model of execution. Because there is no shared memory, the processor connects to its neighbors through a high-speed data link. Messages are sent to a neighbor switch, which in turn forwards that message on to its neighbor until reaching the intended destination. Except for the neighbor connections, processors are isolated and independent of each other.

The processors on the periphery also connect chip-to-chip, thus building up a large processor net. There is no particular topology to the larger net, as a function at each processor allows it to forward a message in the correct direction. Some chip-to-chip connections are not necessarily nearest neighbors, providing short cuts for some of the longer physical distances. The peripheral processors also provide the connections to sensors, actuators, radios, science instruments, and other devices with which the computer system interacts.

This work was done by Kim P. Gostelow of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47894