

Enabling large focal plane arrays through mosaic hybridization

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ABSTRACT

We have demonstrated advances in mosaic hybridization that will enable very large format far-infrared detectors. Specifically we have produced electrical detector models via mosaic hybridization yielding superconducting circuit paths by hybridizing separately fabricated sub-units onto a single detector unit. The detector model was made on a 100mm diameter wafer while four model readout quadrant chips were made from a separate 100mm wafer. The individually fabricated parts were hybridized using a flip-chip bonder to assemble the detector-readout stack. Once all of the hybridized readouts were in place, a single, large and thick silicon substrate was placed on the stack and attached with permanent epoxy to provide strength and a Coefficient of Thermal Expansion match to the silicon components underneath. Wirebond pads on the readout chips connect circuits to warm readout electronics; and were used to validate the successful superconducting electrical interconnection of the model mosaic-hybrid detector. This demonstration is directly scalable to 150 mm diameter wafers, enabling pixel areas over ten times the area currently available.

Keywords: Superconducting Indium Hybridization, Large Focal Plane, Mosaic Bolometer Array

1. INTRODUCTION

The next generation of large-scale science experiments studying the universe will require large format detector arrays containing tens of thousands of pixels¹. These studies will likely include CMB polarization, general evolution of large-scale structure in the universe and other astrophysical phenomena, requiring large focal planes as well as background-limited detector arrays. Currently, there is no existing detector for wavelengths longer than 40 μ m that can meet these science goals. Recognizing this fact and in preparation for the New Worlds, New Horizons (NWNH) decadal survey in astronomy and astrophysics by the National Research Council, a large community of scientists submitted a white paper with clear recommendations, including the need for novel detector array technologies with an order of magnitude or more increase in the format available today².

1.1 Current Detector Architecture

Our current detector architecture has evolved into what is known as the backshort-under-grid (BUG). The BUG architecture is currently in use with the very successful Goddard IRAM Superconducting 2-Millimeter Observer or GISMO instrument^{3,4} as well as having a scaled up version in development for the Primordial Inflation Polarization Explorer or PIPER mission⁵. Both GISMO and PIPER utilize background limited transition edge sensors (TES) as bolometers. They also both employ the BUG, which is a reflective backshort, a separately fabricated part that fits in a cavity behind a membrane that both defines a pixel and contains the TES. GISMO is an array of 8 x 16 pixels on a 2mm pitch with 50 mm walls separating each pixel. This geometry easily accommodates 2-dimensional wiring that fans out to the edge of the chip for wire bonding. PIPER on the other hand, shown in Figure 1, contains 32 x 40 pixels and has a roughly 1mm pitch with similar wall geometry. The pixel density of this array requires 3-dimensional wiring that terminates on a readout substrate after passing through indium bumps for chip-to-chip electrical connectivity.

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A requirement for TES based detectors to work is that all wiring, including the indium cold-weld, needs to be superconducting having reasonable critical current for the application. For instance, PIPER has a requirement on the order of $100\mu\text{A}$. While both GISMO and PIPER require SQUID style multiplexing (MUX) for pixel readout, which are supplied by NIST, the PIPER array is required to be hybridized to the MUX, while GISMO can be wire-bonded to small-scale linear MUX arrays. The evolution of this architecture is prime for scaling up to even larger format detectors.

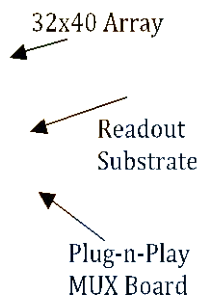


Figure 1. Shown is the PIPER detector package for testing. Here the 32×40 array is hybridized to a simple readout substrate that fans out for wire-bonding to linear MUX's.

To meet the goals stated earlier, that is to develop detector focal planes with many thousands of pixels, a scheme is required that scales up the detector while still being able to read them. The basic scheme would involve straight scaling of both detector and MUX, which would lead to significant increases in cost and development time. However, scaling up the detector array and mosaic tiling the existing MUX architecture, while technically difficult, could yield a more elegant and cost effective approach. Here we demonstrate a technology required to produce space-worthy, far-infrared to sub-millimeter, highly sensitivity bolometer arrays on a scale never before demonstrated. This work establishes the ability to increase detector array formats by an order of magnitude beyond what is currently available⁶ through the use of a novel mosaic hybridization process.

2. METHODS

We utilize standard micro-fabrication techniques to produce a model detector array and the readout quadrant chips. The circuits produced on these chips were designed to test all interfaces between the indium, the readout substrate and the detector array. The basic circuit starts on the substrate with the under-bump-metal (UBM), continues to the indium bump and subsequently on to the landing-pad-metal (LPM) on what is the bottom of the detector array. At this point the circuit is shorted by the LPM back to another set of indium bumps for the return path via the UBM.

2.1 Fabrication

The detector array is made from a 100mm diameter single crystal silicon wafer. The part of the circuit on the detector is comprised of a single layer of d.c. sputtered molybdenum nitride (Mo_2N) and is patterned on the bottom side of the wafer such that it simply acts to short out the circuit from the substrate. This layer is also patterned to receive the indium bumps from the substrate, including the electrically active bumps and those that are purely for mechanical strength and thermal conduction. This material was chosen as the landing-pad-metal primarily because it is a superconductor with a relatively high transition temperature, about 7 Kelvin. Also, molybdenum nitride has a stable surface morphology and is a well-known diffusion barrier⁷. To define the detector geometry we use deep reactive ion etching (DRIE) to transfer a pattern completely through the wafer. This pattern defines the outer frame of the detector as well as each "pixel." A pixel in this sense is a cavity on a pitch of approximately 1 mm, having walls $60\mu\text{m}$ wide between pixels. The detector model is an array of 32×40 of these pixels with the perimeter frame ranging from slightly more than half a millimeter to slightly more than one millimeter wide. The patterned molybdenum nitride resides on the walls between each pixel as well as all along the frame of the detector model.

A full set of readout quadrant chips are fabricated on a single 100 mm diameter single crystal silicon wafer. Prior to any metallization, an insulating layer of 2000Å of SiO₂ is grown on the wafers. The circuit traces that run from edge bond pads to pixel locations are the same type of molybdenum nitride used on the detector, and for similar reasons. This single layer also acts as the under-bump-metal. On top of the UBM and patterned to match up with the LPM, 10 µm of indium is deposited in a lift-off process. There is a “forest” of indium bumps that run around the perimeter of the detector footprint whose primary role is mechanical strength and thermal conduction. This forest however prevents a wiring fan-out to all pixels. Consequently only 64 pixels of 1280 are capable of being readout with this model. The completed substrate is then diced and prepared for hybridization.

2.2 Plasma Cleaning

Standard metallization processes often employ in situ cleaning steps under vacuum conditions that enhance the adhesion or electrical contact between metallic layers. We employ this technique when depositing the indium on top of the molybdenum nitride on the substrate (i.e., the UBM). However, when the substrate is hybridized to the detector, the indium on the substrate essentially cold-welds to the molybdenum nitride on the detector. This process is done in a cleanroom, in air, and it is not possible to do any further processing of the parts while they are on the tool that bonds them together.

When exposed to air at room temperature, indium will readily oxidize, forming a thin “crust” of In₂O₃. This layer of indium oxide can result in two problems, the first being poor adhesion to the LPM. The forces from bonding can rupture a surface film, thereby allowing indium to contact the LPM resulting in good adhesion, however In₂O₃ tends to resist rupturing. The second problem is that In₂O₃ can prevent a barrier to electrical conduction and inhibit a superconducting joint. In fact In₂O₃ has been shown to exhibit a superconductor-insulator-transition effect⁸, although being such a thin surface film, will present a very low critical current.

To overcome these limitations we plasma clean each chip just prior to hybridization using a March CS-1701 plasma cleaning system. For the substrates, we apply r.f. power to a nitrogen-rich, reducing gas mixture. The plasma has the effect to reduce the indium-oxide, which is then replaced by indium-nitride in a self-limiting process. The indium nitride ruptures more readily than the In₂O₃ and enables a good electrical joint between the indium and the LPM. If the indium surface is merely reduced, an oxide will re-grow as soon as the chip is removed from vacuum. The indium nitride layer inhibits this growth allowing for time to complete the hybridization process.

To develop our plasma clean on the indium we used ellipsometry to track the surface film on the indium. We did not calculate thickness directly, but merely tracked the Delta for each measurement. Delta is a simple calculation based on the polarization angles specific to a film and its substrate. It is used to make a measurement of thickness or index of refraction in conjunction with other measurements. As it is directly proportional to thickness, it is a good indicator by itself of the film and when measuring native oxide on indium, the lower the value of Delta, the thicker the In₂O₃ film. In Figure 2 we look at a sample of untreated indium alongside a sample of indium that has received the plasma treatment, and track them both over a long period of time. You can see that the untreated sample has a Delta value that is about 128, which corresponds to the native In₂O₃, and stays at this value over time. The plasma treated sample, however, has a large increase in Delta just after plasma treatment indicating that we have removed the native oxide. Initially, the Delta of this sample drops a little due to removing the sample from the vacuum chamber, as oxygen will attach to indium nitride⁹, however it plateaus over a long period of time well above the control sample due to the passivating effect of the indium nitride.

To prepare the other side of the cold weld joint, that is the molybdenum nitride that makes up the LPM on the detector array, we use a different plasma clean. This process is intended to physically remove a few layers in preparation for bonding. To clean the surface of the molybdenum nitride we use the same reactive ion etch system operating at moderate power with a gas mixture designed for sputtering. After plasma cleaning, all parts are stored in a nitrogen purged dry-box until ready for bonding. The bonding tool itself is purged with nitrogen during the hybridization process.

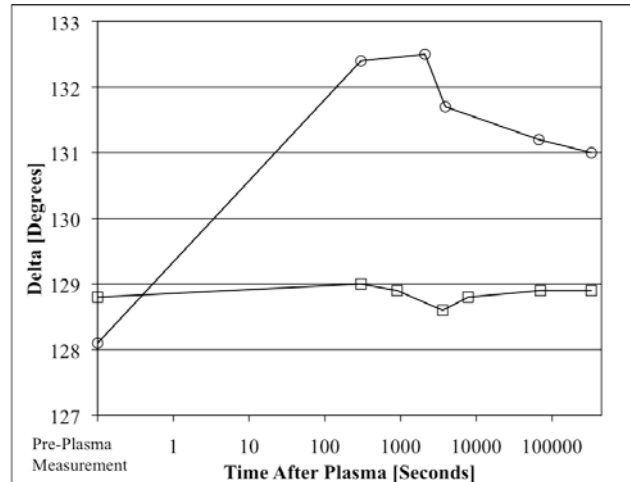


Figure 2. This plot tracks the values of Delta taken from ellipsometry measurements from a control sample (squares), and a plasma cleaned sample (circles). The low Delta value of the control indicates the presence of native oxide. The plasma-cleaned sample has a large increase in Delta, which dips upon venting, but plateaus higher than the control due to the passivating effect of the indium-nitride.

2.3 Hybridization

A flip-chip bonder from Smart Equipment Technology, formerly SUSS, was used to perform the hybridization between the substrate and the detector array. This tool allows for alignment between the two parts to within $\pm 2 \mu\text{m}$. The combined substrates contain over 200,000 indium bumps, in which over 95% are for mechanical attachment between the substrate and the detector as well as thermal conduction, which is poor once the indium is superconducting. We utilize a thermocompression cycle that applies 0.4 gram-force per bump to the parts. The compression of the indium bumps, as seen in Figure 3, is typically slightly more than 50%. A laser leveling routine is employed to ensure a high level of parallelism between the chips just prior to bonding. We can achieve $\pm 1 \mu\text{m}$ of parallelism across a full array. After bonding we anneal the hybrid in a vacuum oven at 120°C for 18 hours. This creates an alloying effect between the indium and molybdenum nitride, which enhances the cold weld joint both mechanically and electrically. Hybrid parts that have been pull-tested indicate our hybrid process can exceed 100 pounds of force¹⁰.

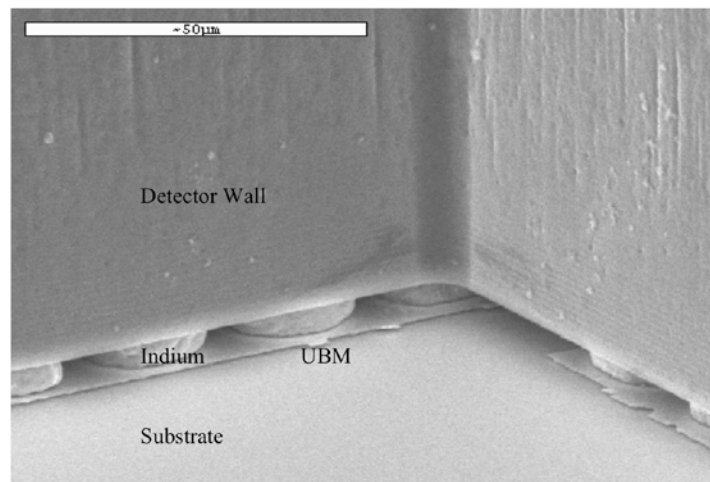


Figure 3. Scanning Electron Microscopy image post hybridization. The view shows a close-up of one corner of a pixel. Visible in the image are the detector wall, substrate with under-bump-metal (UBM) and the indium itself after approximately 50% deformation. Not visible due to the angle, is the landing-pad-metal (LPM).

The hybridization plan for a single completed part is an involved process. Overall, five alignments and thermocompression cycles are needed to make a finished part. The process starts off with aligning the detector array on a custom vacuum plate designed to hold a large array while transmitting the force through the detector walls. This custom part is also designed to handle detector arrays with membranes¹⁰. The readout quadrants are then hybridized one at a time to build up the mosaic. When all of the quadrants are in place, one more piece of silicon is glued to the stack. This solid piece ties all the quadrants together for rigidity. The FC 150 is used for this step to ensure alignment and control the epoxy gap, as well as to cure the epoxy. The gap between the quadrants after hybridization is equivalent to the width of the dicing saw that cuts the substrate after fabrication, which is about 200 μ m.

2.4 Cold Testing

After hybridization the parts are mounted and wire-bonded in a package for cold testing. We are able to wire-bond directly to the molybdenum nitride on the substrate. A successful circuit needs to prove superconducting with adequate critical current in order to be useful and considered successful. To get to the needed temperatures, a simple dewar was used that allowed for pumping on a liquid helium bath. The package was lowered directly into the liquid helium. A Linear Research bridge was used to measure the resistance of each channel connected, while temperature was monitored using a Lakeshore bridge. Data was recorded using Labview software. Using a 4-wire measurement configuration each channel was monitored to see that it went to the lowest reading of the bridge, which corresponded to a value of 0.01 m Ω , this value was taken to indicate a superconducting circuit.

3. RESULTS

Electrically, we have proven a superconducting path from the under-bump-metal, to the indium bumps, to the landing-pad-metal and back to the substrate via a completely new path. Figure 4 shows representative data for the metal systems comprising the circuit of a mosaic hybrid. The superconducting transition of the molybdenum nitride at 6.8 Kelvin is consistent with Mo₂N¹¹. Also shown in Figure 4 is the superconducting transition of the indium at 3.4 Kelvin, which is consistent with bulk indium¹². The data shown in Figure 4 were taken at a measurement range of 2 Ω and an excitation of 2mV indicating a critical current of at least 1mA, sufficient for our PIPER project as well as future missions. This data indicates that we have successfully made a superconducting cold-weld between the indium and the LPM, as well as the indium-molybdenum nitride joint on the substrate. The plasma cleaning process on large-format-arrays produced from the mosaic build process have yielded a successful pixel rate of 91% of testable channels. The failure rate is confined to the corners of the array, which are thought to be due to non-uniform plasma over large areas. This limitation can easily be overcome with a more uniform reactive ion etching system.

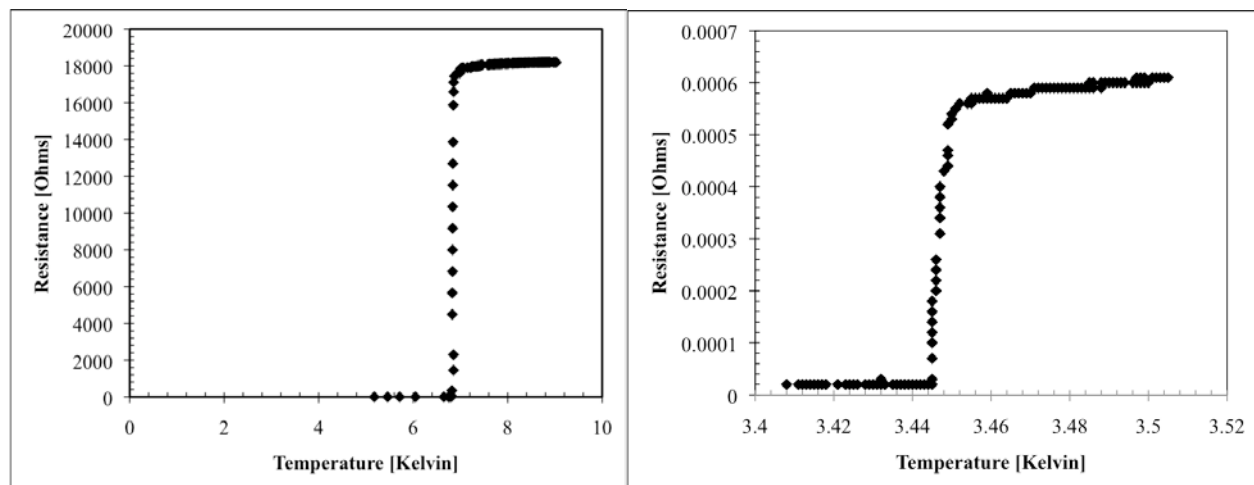


Figure 4. Left: A plot of resistance versus temperature that reveals the critical temperature for the transition from normal metal to superconductor for our molybdenum nitride film. The resistance below the T_c is not zero at this point, as the indium has not yet gone through its transition. Right: A plot of resistance versus temperature that reveals the critical temperature for the transition from normal metal to superconductor for our indium. The overall circuit is superconducting at this point as the resistance is pegged at the lowest possible reading of 0.01 m Ω .

From a mechanical perspective we have successfully built arrays by the mosaic hybridization process. Figure 5 shows the build in various stages as well as a completed detector array with readout electronics. Our hybridization plan accurately built the array by aligning four readout chips on a single detector chip having a grid structure with walls only $60\text{ }\mu\text{m}$ thick. The gap between substrate and detector is a useful metric to determine if a good bond has been made, as it is a good estimate of the final indium bump height and indicates how much the bumps were compressed. Also, when measured across an array it can indicate uniformity in compression or any issues related to the bowing of parts. In our tests, the final gap measurement for all four quadrants was on average $4.1\text{ }\mu\text{m} \pm 0.98\text{ }\mu\text{m}$, indicating an average compression of $5.4\text{ }\mu\text{m}$.

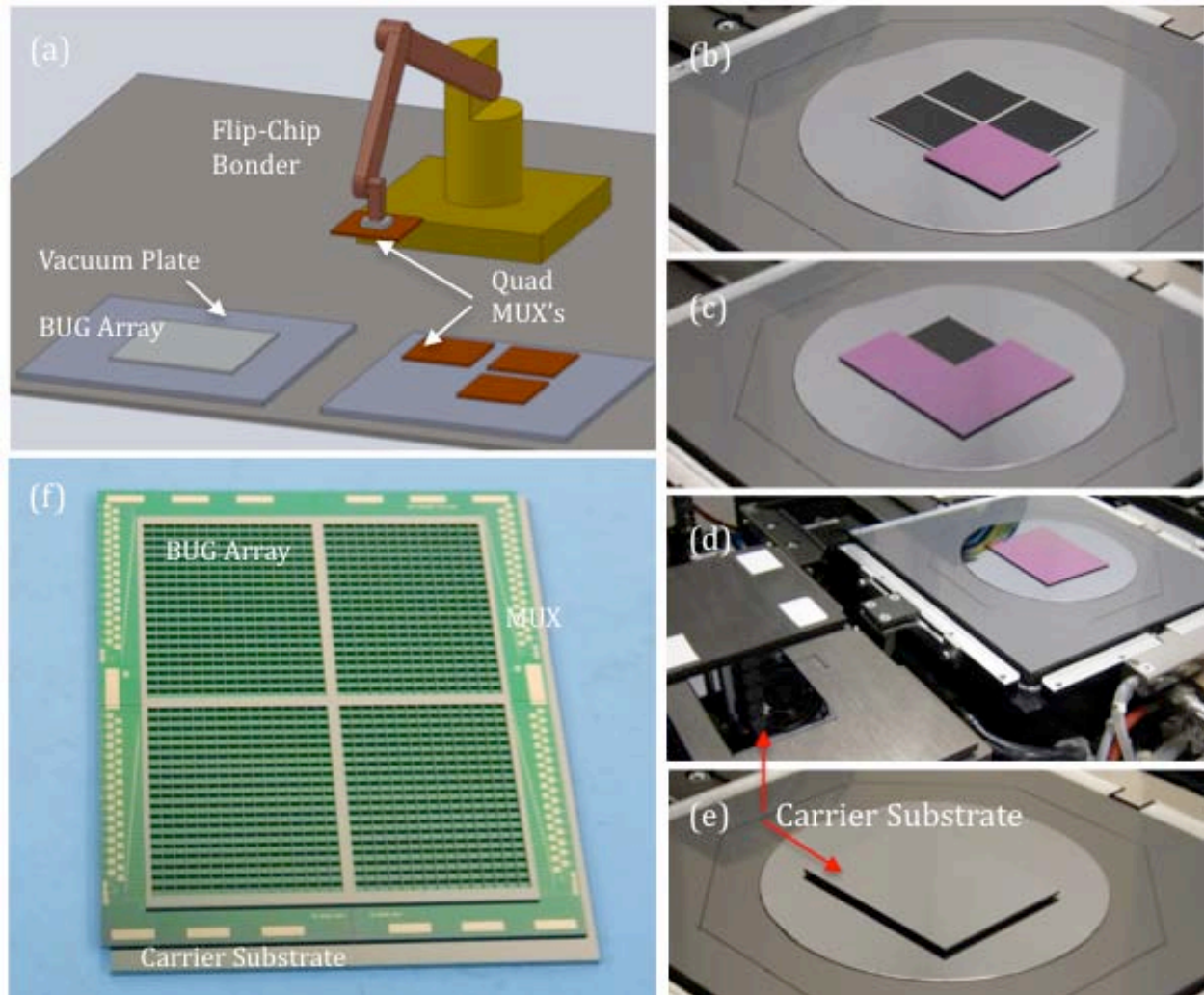


Figure 5. The sequence above illustrates the mosaic build process. (a) is a sketch of the assembly process, showing how the FC150 arm picks and places mosaic quadrants of readout chips onto a single BUG array, oriented facedown, hybridizing with indium bump bonds between each component. Images (b) – (d) are photographs taken of parts on the FC150 vacuum chuck during the assembly process. These show the population of the BUG array with readout quadrants (smaller rectangles). Image (e) shows the final placement of a carrier substrate on top of the readout quadrants, which provides strength to hold the assembly together. At the lower left is a photograph of the front-side of the stack showing the readout quads (with edge wire-bond pads) and the singular detector grid on top. The cross in the grid is solid silicon, one pixel width, used to provide area for indium bumps to hold the quadrants together.

4. SUMMARY

We report a hybridization scheme that will enable large format detectors which utilizes an effective plasma cleaning process for the hybridized parts. The plasma cleaning process has been shown to consistently prepare the indium surface for hybridization. The plasma process also passivates the surface in a way that allows for the indium to sit in air during the hybridization loading and alignment steps, which can take considerable time. This process yielded superconducting circuits with high critical currents, of at least 1mA.

With this mosaic hybridization technology, current detectors can be readily scaled up with only a few design changes. Our demonstration showed that we can tile current sized arrays to build even larger mosaic arrays. We built a mosaic detector and readout quadrants fabricated on 100mm diameter wafers, however this technology is directly scalable to 150mm wafers. In this scenario, the readout quadrants could be the size of the single MUX used for PIPER, while the detector could be produced on a 150mm wafer. The hybridization scheme along with the plasma cleaning is compatible with the needed processes that are required to fabricate a working array with our current background limited detector architecture. With this new technology it is possible to build arrays containing quadrants consisting of 10,000 pixels on a 0.5mm pitch, totaling 40,000 pixels, numbers not currently available for highly sensitive arrays operating at long wavelengths.

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