Compendium of Total Ionizing Dose and Displacement Damage for Candidate Spacecraft Electronics for NASA

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Abstract-- Vulnerability of a variety of candidate spacecraft electronics to total ionizing dose and displacement damage is studied. Devices tested include optoelectronics, digital, analog, linear, and hybrid devices.

Index Terms- Displacement Damage, Optoelectronics, Proton Damage, Single Event Effects, and Total Ionizing Dose.

I. Introduction

NASA spacecraft are subjected to a harsh space environment that includes exposure to various types of ionizing radiation. Long-term exposure to radiation has been known to affect the function of the spacecraft electronics. As a result, flight parts must be tolerant to radiation-induced Total Ionizing Dose (TID) and displacement damage (DD) effects or be mitigated by shielding or other methods to reduce TID and DD effects. Hence, the effects of TID and DD need to be evaluated by test in order to determine risk to spaceflight applications.

The test results presented here were gathered to establish the sensitivity of candidate spacecraft electronics to TID and/or DD damage. Proton-induced degradation, dominant for most NASA missions, is a mix of ionizing (TID) and non-ionizing damage. The non-ionizing damage is commonly referred to as displacement damage (DD). For similar results on single event effects (SEE), a companion paper has also been submitted to the 2012 IEEE NSREC Radiation Effects Data Workshop entitled: "Compendium of Single Event Effects for Candidate Spacecraft Electronics for NASA" by M. O'Bryan, et al. [1]

II. Test Techniques and Setup

A. Test Methods – TID

TID testing was performed using a ^{60}Co source. Dose rates used for testing were between 0.05 and 18 rad(Si)/s.

B. Test Methods – Proton

Proton DD/TID tests were performed at the University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL) using a 76" cyclotron (maximum energy of 63 MeV). Table I lists the proton damage test facilities and energies used on the devices.

TABLE I: PROTON TEST FACILITIES

Facility	Incident Proton Energy, (MeV)
University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL)	6.5-63

C. Test Methods – Electron

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages.

III. Test Results Overview

Abbreviations for principal investigators (PIs) are listed in Table II. Abbreviations and conventions are listed in Table III. Summary of TID and DD test results are listed in Table IV.

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TABLE II
LIST OF PRINCIPAL INVESTIGATORS

Abbreviation	Principal Investigator (PI)
DB	David Batchelor
AB	Alvin Boutte
MiC	Michael Campola
MeC	Megan Casey
DC	Dakai Chen
RL	Raymond Ladbury
JML	Jean-Marie Lauenstein
TO	Timothy Oldham
JP	Jonathan Pellish
EW	Edward (Ted) Wilcox

TABLE III
ABBREVIATIONS AND CONVENTIONS

A = Amp
B_H = Magnetic Hysteresis
BiCMOS = Bipolar – Complementary Metal Oxide Semiconductor
B_{JT} = Bipolar Junction Transistor
B_{OP} = Magnetic Operating Point
B_{RP} = Magnetic Release Point
BV_{dss} = Breakdown Voltage
CMOS = Complementary Metal Oxide Semiconductor
CTR = Current Transfer Ratio
DAC = Digital to Analog Converter
DC-DC = Direct Current to Direct Current
DD = Displacement Damage
DDR = Double-Data-Rate (a type of SDRAM—Synchronous Dynamic Random Access Memory)
DIMM = Dual In-Line Memory Module
DNL = Differential Non-Linearity
DTRA = Defense Threat Reduction Agency
DUT = Device Under Test
$DV_{out/}$ DI_{out} = Output Voltage Load Regulation
ELDRS = Enhanced Low Dose Rate Sensitivity
FET = Field Effect Transistor
FPGA = Field Programmable Gate Array
HBT = Heterojunction Bipolar Transistor
H_{FE} = Forward Current Gain
I_b = Base Current
I_{bias} = Input Bias Current
I_c = Collector Current
I_{ce} = Output Current
IDD = Supply Current
I_f = Input Forward Current
I_{GSS} = Gate Reverse Current
I_{os} = Offset Current
InGaP = Indium Gallium Phosphide
I_{OUT} = Output Current
JFET = Junction Field Effect Transistor
LCC = Leadless Chip Carrier
LDC = Lot Date Code
LDO = Low Dropout
LED = Light Emitting Diode
LDR = Low Dose Rate
LDR EF = Low Dose Rate Enhancement Factor
Loadreg = Load Regulation
MDAC = Multiplying Digital-to-Analog Converter
MeV = Mega Electron Volt
mA = milliamp
MOSFET = Metal Oxide Semiconductor Field Effect Transistor
Mrad = megarad
N/A = Not Available
Op-Amp = Operational Amplifier
PI = Principal Investigator
PSRR = Power Supply Rejection Ratio
REAG = Radiation Effects & Analysis Group
SEE - Single Event Effects
Spec = Specification(s)
TID = Total Ionizing Dose
UCD-CNL = University of California at Davis – Crocker Nuclear Laboratory
V_{bias} = Bias Voltage
V_{ce} = Collector Emitter Voltage
V_{CEsat} = Collector-Emitter Saturation Voltage
VDD =Supply voltage
V_{IH} = High Level Input Voltage
V_{in} = Voltage In
V_{os} = Input Offset Voltage
V_{oso} = Output Offset Voltage
V_{out} = Output Voltage
V_{ref} = Reference Voltage
V_{th} = Threshold Voltage
V_z = Reverse Breakdown Voltage

TABLE IV
SUMMARY OF TID AND DD TEST RESULTS

Part Number	Manufacturer	LDC	Device Function	Technology	PI	Results	App. Spec (Y/N)	Dose rate (rads(Si)/s) or Proton Energy (MeV)	Degradation Level (krad(Si)) or Proton Fluence
Analog to Digital / Digital to Analog Converters									
AD7847SQ	Analog Devices	1006C	12-bit MDAC	CMOS	JP	All devices passed up to 20 krad(Si). The Digital Nonlinearity parameter tested outside of the datasheet spec for one device at 5 krad(Si), but was within spec for the remainder of testing.	N	0.01	> 20
HELI-X	Tower Jazz	N/A	Analog to Digital Converter Track and Hold Circuit	CMOS	MeC	All parts remained functional to the final dose 1.5 Mrad(Si) for two parts and 3 Mrad(Si) for two others), but did see an increase in power supply current.	Y	0.9 - 49	> 1500
Flash Memory									
K9F8G08UOM	Samsung	0807	Flash Memory	CMOS	TO	Passed at 400 krad(Si), failed at 500 krad(Si).	N	30	200 < x < 500
M379T2863FB3-CF7	Samsung	N/A	DDR2 Memory	CMOS	RL	Operational Currents IDD increased monotonically for biased parts but showed little change for parts irradiated unbiased. Functional failures occurred at 900 krad(Si) (unbiased) and 1 Mrad(Si) (biased). See Table IV.	N	30	125<IDD5B<150, 175<IDD3P<200, 225<IDD3N<225. 225<IDD4W<225, 350<IDD4R<400
MT29F16G08ABABA	Micron	1006	Flash Memory	CMOS	TO	Errors reset at 75 krad(Si), functional failure at 100 krad(Si).	N	30	75 < x < 100
Miscellaneous									
53111	Micropac	1105	Solid State Relay	Hybrid	JP	All parameters passed to tested level.	N	63 MeV	> $1x10^{12}$ proton/cm^2
A3PE1500	Microsemi	Various	FPGA	CMOS	EW	Evaluating new testing method. Parts showed 10% degradation at 20 krad(Si).	N	1.6	20 < x < 25
AD8465	Analog Devices	1046	Comparator	Bipolar XFCB2	JP	Part passed all tested parameters up to and including the final dose step.	N	17	> 80
FET Array Test Chip	Tower Jazz	N/A	FET Array Test Chip	CMOS	MeC	All parts survived up to 1 Mrad(Si). One part experienced a functional failure at 3 Mrad(Si).	Y	0.9 - 7	1000 < x < 3000
MAX9202ESD	Maxim	1041	Comparator	Bipolar	JP	Low measurement fidelity on input offset voltage data (see report), but other parameters passed up to and including the final dose step.	N	10	> 20
NC7SZ74	Fairchild Semiconductor	B1021AK	Flip-Flop	CMOS	JP	All parameters passed up to 20 krad(Si).	Y	0.01	> 20
OC100HG	Voltage Mult Inc.	1028	High-voltage optocoupler	Infrared Emitter	MeC	The CTR degraded for V_{in} = 1000 V and V_{in} = 10000 V, but remained within specification to a fluence of $2x10^{12}$ p/cm^2.	N	63 MeV	> $2x10^{12}$ proton/cm^2
OMH3075s	Optek	M0904	Hall-Effect Switch	Linear Bipolar	DB	Degradation <10% in B_{OP}, B_{RP} & B_H, all other parameters within spec.	Y	10	> 20

Part Number	Manufacturer	LDC	Device Function	Technology	PI	Results	App. Spec (Y/N)	Dose rate (rads(Si)/s) or Proton Energy (MeV)	Degradation Level (krad(Si)) or Proton Fluence
UC1524A	Unitrode/Texas Instruments	0620A	Advanced Regulating Pulse Width Modulator	Bipolar	JP	All parameters passed up to 20 krad(Si).	N	0.01	> 20
UC1526/883B	Texas Instruments	0952A	Regulating Pulse Width Modulator	Bipolar	JP	I_{os} tested outside of the datasheet spec between 5 and 10 krad(Si), while V_{out} and Loadreg tested outside of spec between 10 and 15 krad(Si) and I_{bias} between 15 and 20 krad(Si).	Y	0.01	$5 < I_{os} < 10$ $10 < V_{out} < 15$ 10 <Loadreg < 15 $15 < I_{bias} < 20$
UT54ACS08	Aeroflex	0907	Quadruple 2-input AND Gate	CMOS	MeC	All parts remained functional to 6 Mrad(Si), but the low-to-high propagation delay exceeded the specification at that dose level.	N	0.45 - 10	3000 < x < 6000
Operational Amplifiers									
AD524	Analog Devices	0944	Instrumentation Amplifier	Bipolar	RL	V_{os} exhibited bimodal response, with some parts failing <5 krad(Si) and others passing up to 50 krad(Si). V_{oso} response also bimodal, but passed spec.	Y	0.01	$2.5<V_{os}<5$
AD648	Analog Devices	0953A	Quad Operational Amplifier	Bipolar	JP	I_{bias} for all devices showed radiation induced degradation outside of the datasheet spec between 2 and 5 krad(Si) while the I_{os} tested outside of the spec provided by the datasheet pre-irradiation.	Y	0.01	$2 < I_{bias} < 5$
AD823AR	Analog Devices	0953	Operational Amplifier	Bipolar	JP	I_{os} appeared to have radiation induced degradation outside of the datasheet spec between 5 and 10 krad(Si).	Y	0.01	$5 < I_{os} < 10$
AD847SQ	Analog Devices	0937B	Operational Amplifier	Bipolar	AB	The PSRR for the biased devices was the only out of spec between 5 and 7 krad(Si).	Y	0.01	5 < PSRR < 7
CA308OAS3	Intersil	H043AH7	Operational Amplifier	Bipolar	JP	All parameters passed up to 25 krad(Si).	Y	0.01	> 25
LTC2054	Linear Technology	1047T	Operational Amplifier	Bipolar	JP	All parameters passed up to 30 krad(Si).	Y	0.01	> 30
OP15S	Analog Devices	0401	Operational Amplifier	Bipolar	RL	All devices were functional past a total dose of 50 krad(Si). I_{os} and V_{os} out of spec between 10 and 15 krad(Si).	Y	0.01	$10 < I_{os} < 15$, $10 < V_{os} < 15$
OP200	Analog Devices	0932B	Dual Operational Amplifier	Bipolar	JP	I_{bias} in both channels of the unbiased devices tested outside of the datasheet spec between 17.5 and 20 krad(Si) and V_{os} of channel A tested out of spec after irradiation between 13 and 15 krad(Si) for the unbiased and between 17.5 and 20 krad(Si) for the biased. All other parameters passed after irradiation up to 20 krad(Si).	Y	0.01	$17.5 < I_{bias} < 20$ $13 < V_{os} < 15$

Part Number	Manufacturer	LDC	Device Function	Technology	PI	Results	App. Spec (Y/N)	Dose rate (rads(Si)/s) or Proton Energy (MeV)	Degradation Level (krad(Si)) or Proton Fluence
OP462HRU	Analog Devices	1012	Dual Operational Amplifier	Bipolar	JP	All parameters passed up to 20 krad(Si).	Y	0.01	> 20
RH1078MH (TO-5 Metal Can)	Linear Technology	0325A	Precision Operational Amplifier	Bipolar	DC	0.5 mrad(Si)/s: 3 biased, 2 unbiased parts exceed spec for V_{os} after 25 krad(Si). 1 mrad(Si)/s: 2 parts each biased and unbiased exceed spec for V_{os} after 20 krad(Si). Test in progress.	Y	0.001	$10<V_{os}<20$
								0.0005	$15<V_{os}<25$
RH1078MW (Flatpack)	Linear Technology	0741A	Precision Operational Amplifier	Bipolar	DC	Devices within spec. Test in progress.	Y	0.001	>20
								0.0005	>25
RHF310 (Ceramic Flat-8)	ST Microelectronics	30849A	Operational Amplifier	Bipolar	DC	Parameters within spec for parts irradiated at 5 mrad(Si)/s after 5 krad(Si). 1 mrad(Si)/s irradiation currently in progress.	N	0.0005	>5
RHF43B (Ceramic Flat-8)	ST Microelectronics	30820A	Operational Amplifier	Bipolar	DC	Parameters within spec for parts irradiated at 10, 5 & 1 mrad(Si)/s after 100, 30 & 20 krad(Si).	N	0.001	>100
								0.005	>30
								0.001	>20
Power MOSFETs									
CMF20120D	Cree	A11011	n-type Silicon Carbide Power MOSFET	CMOS	MeC	The breakdown voltage (BV_{dss}) went out of spec (1200 V) at 250 krad(Si), and the threshold voltage (V_{th}) dropped below 1 V at 350 krad(Si). For all cases, the parts biased ON during irradiation exhibited the most degradation.	N	0.9 - 14	200 < x < 250
Si7431DP	Vishay	AB W08B	Power MOSFET	Power p-type TrenchFET®	JML	On-state biased samples out of spec: $25 < V_{th} < 30$ krad(Si); off-state & grounded samples: $50 < V_{th} < 75$ krad(Si).	N	0.09 - 17	$25 < V_{th} < 30$
SUM45N25	Vishay	T86T CF	Power MOSFET	Power n-type TrenchFET®	JML	On-state biased samples out of spec: $5 < V_{th} < 7.5$ krad(Si); $10 < I_{DSS}$, $BV_{dss} < 12.5$ krad(Si); some room-temp annealing. Off-state & grounded samples all within spec after 15 krad(Si).	N	0.04 - 8.6	$5 < V_{th} < 7.5$
Transistors									
2N2222	Semicoa	0743	Silicon NPN Switching Transistor	Bipolar	MeC	These parts were irradiated to 1 Mrad(Si), forward current gain (h_{FE}) went out of spec 100 krad(Si).	N	42	30 < x < 100
2N2222AJSR	Semicoa	1364	BJT	Bipolar	DC	At 0.01 rad(Si)/s, current gain at low injection levels (IC=1 and 0.1 mA) failed parametrically between 35 and 40 krad(Si). The LDR EF = ×3.9 after 100 krad(Si).	N	0.01	$35 < h_{FE} \leq 40$

Part Number	Manufacturer	LDC	Device Function	Technology	PI	Results	App. Spec (Y/N)	Dose rate (rads(Si)/s) or Proton Energy (MeV)	Degradation Level (krad(Si)) or Proton Fluence
2N2369	Semicoa	1934	BJT	Bipolar	DC	All parameters are within spec up to 100 krad(Si). Minimal LDR EF.	N	50	50 >100
								0.01	0.01 > 100
2N2857	Semicoa	1523	BJT	Bipolar	DC	At high dose rate, all parameters within spec up to 100 krad(Si). Low dose rate in progress.	N	50	50 >100
								0.01	0.01 > 17
2N2907AJSR	Semicoa	1324	BJT	Bipolar	DC	Low dose rate in progress. LDR EF = ×1.78 after 100 krad(Si).	N	0.01	$40 < h_{FE} \leq 50$
2N5153	Semicoa	1013	BJT	Bipolar	DC	All parameters are within spec up to 100 krad(Si). Minimal LDR EF.	N	50	50 >100
								0.01	0.01 > 100
2N5154	Semicoa	1023	BJT	Bipolar	DC	All parameters are within spec up to 100 krad(Si). LDR EF = x4.21 after 100 krad(SI).	N	50	50 >100
								0.01	0.01 > 100
BFR92A	Philips/NXP	1027	NPN Transistor	Bipolar	JP	All parameters passed up to 20 krad(Si).	Y	0.01	> 20
BFT92	Philips/NXP	0950	PNP Transistor	Bipolar	JP	All parameters passed up to 20 krad(Si).	Y	0.01	> 20
JANTXV2N2222AUB	Microsemi	0951	NPN Transistor	Bipolar	JP	All parameters passed up to 20 krad(Si).	N	0.01	> 20
JANTXV2N2907AUB	Semicoa	1020	PNP Transistor	Bipolar	JP	All parameters passed up to 20 krad(Si).	N	0.01	> 20
JANTXV2N3501UB	Microsemi	1007	NPN Transistor	Bipolar	JP	All parameters passed up to 20 krad(Si).	N	0.01	> 20
SFT5015-39TXV	Solid State Devices	1032	NPN Transistor	Bipolar	JP	Gain = 0 at 25 krad(Si) for unbiased parts.	N	0.01	20 < x <25
SFT5015-4TXV	Solid State Devices	1016	NPN Transistor	Bipolar	JP	Gain = 0 at 25 krad(Si) for unbiased parts.	N	0.01	20 < x <25
SFT5094-4TXV	Solid State Devices	1007	PNP Transistor	Bipolar	JP	All DUTs within spec for all parameters at highest dose tested (25 krad(Si)). Some reduction in gain with dose, but all parts still within spec at high does level (25).	N	0.01	20 < x <25
Voltage References / Voltage Regulators									
AD586T	Analog Devices	0505A	Voltage Reference	Bipolar	JP	Output voltage increased beyond spec after 5 krad(Si).	N	10	$5 < V_{out} < 10$
AD589	Analog Devices	0445	Voltage Reference	Bipolar	JP	Part passed all tested parameters up to and including the final dose step.	N	10	> 47
LM117HRQMLV (TO-39 metal can)	National Semiconductor	7D5867L019	Adjustable Voltage Regulator	Bipolar	DC	LDR enhancement observed for V_{ref} degradation. Parameters within spec after 90, 20, & 15 krad(Si) for the 5, 1, & 0.5 mrad(Si)/s parts.	N	0.005	> 90
								0.001	> 20
								0.0005	> 15
LM136AH2.5QMLV (3-lead TO-46)	National Semiconductor	200746K019	Voltage Reference	Bipolar	DC	Exhibits no LDR EF. Parameters within spec after 100, 20, & 10 krad(Si) for the 5, 1, & 0.5 mrad(Si) devices.	N	0.005	>100
								0.001	>20
								0.0005	>10

Part Number	Manufacturer	LDC	Device Function	Technology	PI	Results	App. Spec (Y/N)	Dose rate (rads(Si)/s) or Proton Energy (MeV)	Degradation Level (krad(Si)) or Proton Fluence
LM317KTTR	Texas Instruments	0608	Positive Voltage Regulator	Bipolar	DC	Parameters within spec after 80, 20, & 15 krad(Si) for the 5, 1, & 0.5 mrad(Si) parts. LDR enhancement observed for parts irradiated at 0.5 & 1 mrad(Si)/s after 20 krad(Si).	N	0.005	>80
								0.001	>20
								0.0005	>15
LTC1877	Linear Technology	1033, 1132	Voltage Regulator	CMOS	JP	Biased samples out of spec for several parameters at 20 krad(Si).	N	30	1st parametric failure at 5
LT1009IDR	Texas Instruments	0606	Internal Reference	Bipolar	DC	Exhibits no LDR EF. Parameters within spec after 100, 30, & 15 krad(Si) for the 5, 1, & 0.5 mrad(Si) parts.	N	0.005	>100
								0.001	>30
								0.0005	>15
LTZ1000	Linear Technologies	0851	Ultra Stable Voltage Reference	Bipolar	MiC	Application circuit stayed within spec for LDR EF.	Y	0.01	> 50
RH1009MH (TO-46 can)	Linear Technology	0829H	Voltage Reference	Bipolar	DC	Exhibits LDR EF after 20 krad(Si) for devices irradiated at 5 & 1 mrad(Si)/s. 5 mrad(Si)/s TO-46 cans: $80 < V_z < 90$ krad(Si).	N	0.005	$80 < V_z < 90$
								0.001	>20
								0.0005	>10
RH1009MW (Flatpack)	Linear Technology	0649A	Voltage Reference	Bipolar	DC	Exhibits LDR EF after 15 krad(Si) for devices irradiated at 5 & 1 mrad(Si)/s. 5 mrad(Si)/s Flatpacks: $100 < V_z < 120$ krad(Si).	N	0.005	$100 < V_z < 120$
								0.001	>20
								0.0005	>10
RH1021CMW-5 (TO-5 can)	Linear Technology	9783A	Precision Voltage Reference	Bipolar	DC	LDR EF observed for parts irradiated at 5 mrad(Si)/s after 30 krad(Si). 5 mrad(Si) (TO-5): $90 < V_z < 100$ krad(Si).	N	0.01	>50
								0.005	$80 < V_z < 90$
								0.001	>20
								0.0005	>10
RH1021CMW-5 (Flatpack)	Linear Technology	0123A	Precision Voltage Reference	Bipolar	DC	Parameters within spec after 100, 20, & 10 krad(Si) for 5, 1, & 0.5 mrad(Si)/s.	N	0.005	>100
								0.001	>20
								0.0005	>10
RHFL4913ESY332 (TO257)	ST Microelectronics	30828A	Voltage Regulator	Bipolar	DC	Parameters within spec for parts irradiated at 10, 5 & 1 mrad(Si)/s after 100, 30 & 20 krad(Si).	N	0.001	>100
								0.005	>30
								0.001	>20
RHFL4913KP332 (Flat-16)	ST Microelectronics	30814B	Voltage Regulator	Bipolar	DC	Parameters within spec for parts irradiated at 10, 5 & 1 mrad(Si)/s after 100, 30 & 20 krad(Si).	N	0.01	>100
								0.005	>30
								0.001	>20
TL750L05CDR	Texas Instruments	0605	LDO Positive Voltage Regulator	Bipolar	DC	Exhibits LDR EF for functional failures. Degradation level shows initial failure dose levels.	N	0.01	$50<V_{out}<60$
								0.005	$35<V_{out}<40$
								0.001	$10<V_{out}<15$
								0.0005	$7.5<V_{out}<10$
TL750M05CKTRR (TO263-3)	Texas Instruments	0707	LDO Positive Voltage Regulator	Bipolar	DC	V_{out} failure levels (I_O = 10 mA): 5 mrad(Si)/s: $70 < V_{out} < 80$ krad(Si). 1 mrad(Si)/s: > 20 krad(Si) 0.5 mrad(Si)/s: > 15 krad(Si).	N	0.005	$70<V_{out}<80$
								0.001	>20
								0.0005	>15

IV. Test Results and Discussion

As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [3] describing in further detail, test method, TID conditions/parameters, test results, and graphs of data.

A. CMF20120D/ n-channel enhancement mode Silicon Carbide MOSFET/CREE

The CMF20120D is a n-channel enhancement mode Silicon Carbide MOSFET manufactured by CREE using their Z-FET technology. The samples in this test were surface-mounted on copper boards having pins designed to plug into wire wrap sockets. The parts were irradiated using a ^{60}Co source, at varying dose rates of 500-1000 rad(Si)/min during the day and 5-25 rad(Si)/min overnight, to a total dose of 400 krad(Si). The parts were tested until the threshold voltage dropped below 1 V (there is no minimum threshold voltage specified for these parts). On the other hand, breakdown voltage deteriorated beyond the minimum 1200 V specification between 200 and 250 krad(Si). After that point, the MOSFETs underwent a one-week room-temperature anneal under bias, with measurements at 24 hours post-anneal, and following the full 168 hour anneal. Parts were then irradiated for an additional 200 krad(Si). They were then subjected to a 168-hour anneal at 100 °C, with measurements only after the full time period. A total of ten MOSFETs were used for this test, nine of which were biased either in an on-state, off-state, or grounded state, with the remaining device used as a control. Specifically, the on-state bias conditions were 20 V on the gate and grounded source and drain; the off-state bias conditions were grounded gate and source and 900 V on the drain; and the grounded bias conditions shorted all pins to ground.

Fig. 1 shows the average threshold voltage for each bias condition and the control as a function of dose. Likewise, Fig. 2 plots the breakdown voltage as a function of dose. All averaged parameters stayed within specification to 400 krad(Si), except the breakdown voltage. After the week long high temperature anneal, all parameters returned to their pre-rad values.

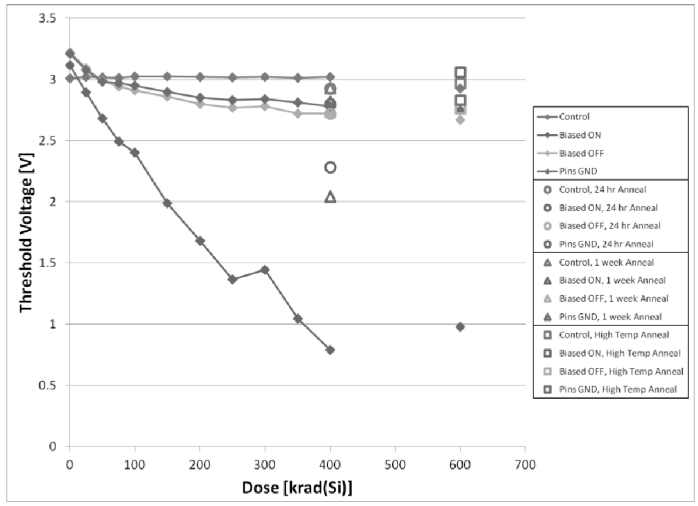

Fig. 1. The average threshold voltage for the CMF20120D as a function of dose.

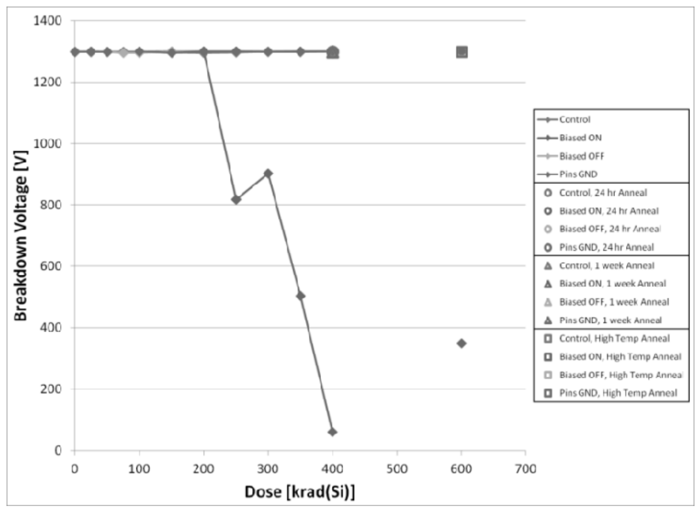

Fig. 2. The average breakdown voltage for the CMF20120D as a function of dose.

B. M379T2863FB3-CF7/Samusung DDR2 Memory DIMM

Samsung 1-Gbit DDR2 DIMMs (part # MV-2V1G4 fabricated with M379T2863FB3-CF7 die) were evaluated for tolerance to TID degradation. The parts were irradiated according MIL-STD 883 Method 1019.8, with the exception that the dose rate was between 5 and 30 rad(Si)/s, rather than 50-300 rad(Si)/s. As each DIMM included 8 DDR2 die, a single DIMM provides some measure of part-to-part variation. One DIMM was irradiated unbiased, while the other was irradiated with a static bias applied to VDD. The unbiased DIMM showed very little degradation in either DC parameters (IDD during operational conditions as defined in Table V) per the JEDEC DDR2 specification [4] or the timing parameters, but failed functionally at 900 krad(Si).

For both biased and unbiased DIMMs, the first dynamic test that failed was the Hammer Read, in which the tester reads repeatedly from the same memory address. This indicates that it is likely that the functional failures arise from weak cells in the memory and are unrelated to the behavior of the DC parameters shown in Table V and Fig. 3.

TABLE V
LIST OF OPERATIONAL CURRENTS

Parameter	Description	Parameter	Description
IDD0	Operating One Bank Active-Precharge	IDD3N	Active Standby
IDD1	Operating One Bank Active-Read-Precharge	IDD4R	Operating Burst Read
IDD2P	Precharge Power-Down (slow exit)	IDD4W	Operating Burst Write
IDD2N	Precharge Standby	IDD5B	Burst Refresh
IDD2Q	Precharge Quiet Standby	IDD6	Self Refresh
IDD3P	Active Power-Down (fast exit)	IDD7	Operating Bank Interleave Read

In contrast, parts irradiated with static bias showed more or less monotonic increase in current drawn, exceeding specified values at ~150 krad(Si) for IDD5B, the Burst Autorefresh Current. (See Fig. 3) Four other operational currents, first IDD3P (~180 krad(Si)), then IDD3N and IDD4W (220 krad(Si)) and finally IDD4R (~275 krad(Si)) also exceeded manufacturer's spec. Functional failure for the statically biased devices occurred at the 1 Mrad(Si) dose step.

For both biased and unbiased DIMMs, the first dynamic test that failed was the Hammer Read, in which the tester reads repeatedly from the same memory address. This indicates that it is likely that the functional failures arise from weak cells in the memory and are unrelated to the behavior of the DC parameters shown in Fig. 3.

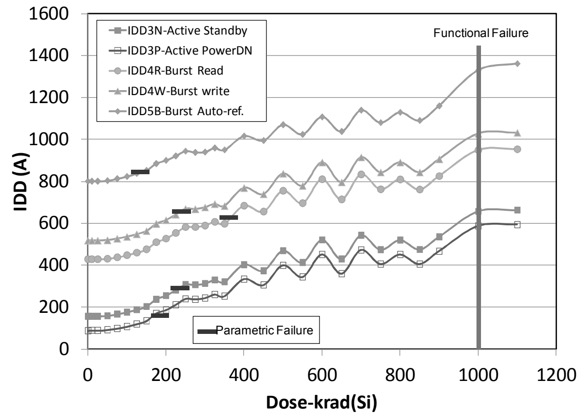

Fig. 3 Although statically biased Samsung DDR2 DIMMs exhibit monotonic degradation in operational supply currents, and 5 parameters exceed manufacturer's specification, functional failure occurred at roughly the same dose as for the unbiased DIMM.

V. SUMMARY

We have presented data from recent TID and proton-induced damage tests on a variety of primarily commercial devices. It is the authors' recommendation that this data be used with caution due to many application/lot-specific issues. We also highly recommend that lot testing be performed on any suspect or commercial device.

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