Large Format Transition Edge Sensor Microcalorimeter Arrays

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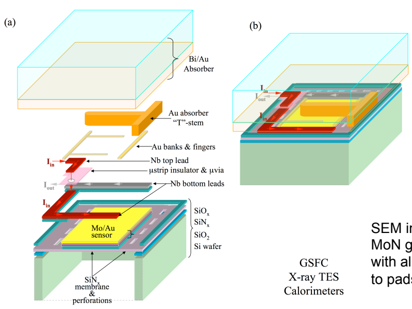
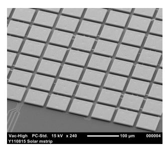
Next Generation X-ray Focal Planes

We have produced a variety of superconducting transition edge sensor array designs for microcalorimetric detection of x-rays. Designs include kilopixel scale arrays of relatively small sensors (~75 micron pitch) atop a thick metal heatsinking layer as well as arrays of membrane-isolated devices on 250 micron and up to 600 micron pitch. We discuss fabrication and performance of microstripline wiring at the small scales achieved to date. We also address fabrication issues with reduction of absorber contact area in small devices.

Exploded view of microcalorimeter process with microstripline wiring

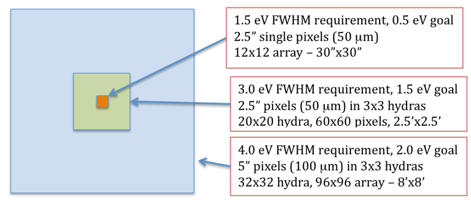


GSFC X-ray TES Calorimeters



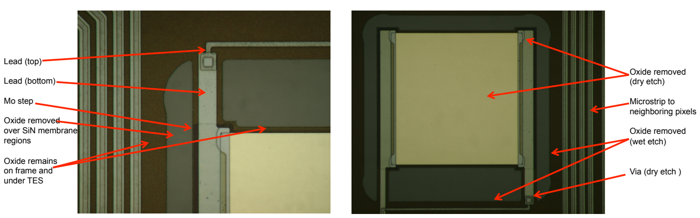
SEM image showing 75 micron pitch array on Cu with MoN groundplane. Kilopixel scale arrays produced with all pixels wired to edge of array. (To wire all pixels to pads requires a much larger chip! ~ 90 mm in dim.)

Example of proposed focal plane in support of NASA Mission Concept: SAHARA

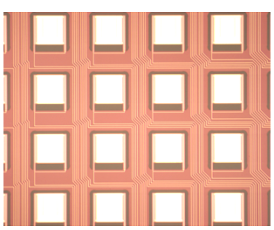


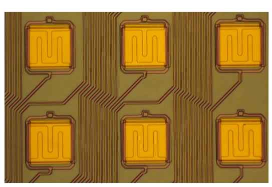
Focal planes with multiple pixel varieties will require:
- Optimization of lead routing for bias uniformity
- Simultaneous detector specifications under same operating conditions
- Heatsinking for variable bias power and high x-ray flux at array center

Micrographs of TES devices after microstrip process is complete

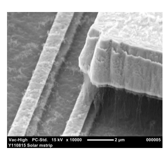


Design variations:
Rerouted wiring and via locations for compactness, symmetry, and magnitude / distribution of "self" field
Normal metal features (edge banks, stripes, stem) varied
Absorber thickness / material (dominant source of heat capacity in these devices)





TES with microstrip surround wiring. Top conductor creates a loop around the entire device.



SEM detail – 1.5 micron wide top conductor running under cantilevered Au absorber

Microstrip wiring enables new geometries to tune self fielding effects. Designs with a superconducting loop around each detector (center) show a different Ic(B) periodicity than asymmetric wiring (as in the left hand side) which applies a larger, less uniform field. (Right hand side SEM) Microstrip with 4 micron pitch (2.5 micron bottom conductor) achieved greater than 1 mA critical current and low crosstalk to neighboring pixels.

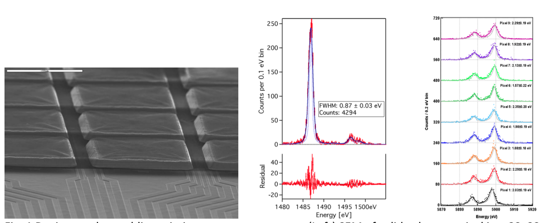
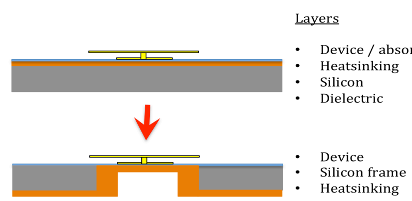


Fig. 1 Device results enabling mission concept prototypes (Left) SEM of solid substrate pixel in a 32x32 array format on 75-micron pitch (developed for solar physics). (Center) Spectra of single pixel (0.87 eV at 1.5 keV). (Right) "Hydra" microcalorimeter with 2.2 eV at 6 keV in the TES in all nine absorbers.

Proposal for fabrication reordering in solid substrate TES microcalorimeter devices



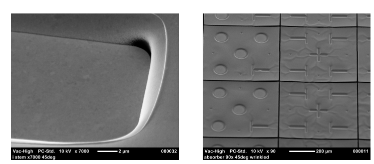
Replace initial heatsink layer deposition with deep etch under each device and subsequent thick metal deposition

OPTIMIZE HEATSINK FOR ARRAYS WITH MULTIPLE DEVICE TYPE: Through shadowmasking, common devices will have a mutual heatsink while different types of devices could have some isolation among metallic heatsinking regions. Front to back heatsinking can be achieved with deep etched through-wafer vias outside of device region of the array

Advantages: Fabrication is simplified by removing heatsinking layer (which has a higher surface roughness)
Enables co-existence of "solid substrate" and "membrane" devices in same focal plane, as needed.
Allows examination of possible changes to thermal crosstalk channel in solid substrate. For example frontside cuts to suppress crosstalk through the dielectric.

Possible issues: Achieving equivalent film quality (RRR) on DRIE sidewall and around corner.
Geometry more complex if superconducting ground plane is used / needed

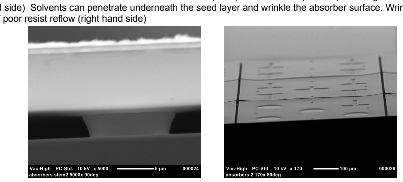
Absorber Integration in Small TES or Small Absorber Stem Devices



Reduction in TES device size requires reduction in stem feature size. Further, the fraction of total absorber area must remain Small to avoid hot phonon loss.

Photoresist sacrificial layer is reflowed to promote sidewall coverage of metal seed layer for subsequent electroplating of thick absorber films

Reflow of resist into narrow stems and around corners can cause pile up that results in poor step coverage of the metal seed layer. (left hand side) Solvents can penetrate underneath the seed layer and wrinkle the absorber surface. Wrinkles emanate from regions of poor resist reflow (right hand side)



Thick Au absorber, left hand side, (~3 micron) yielded without care in reflow / seed layer deposition

Thinner Au (0.8 micron, right hand side), required care in reflow, multiangle seed layer deposition to achieve flat film

Film stress in thin Au can still cause delamination from photoresist sacrificial layer when cycled to high temperatures