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High Temperature Boost (HTB) Power Processing Unit (PPU) Formulation Study

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January 2013

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High Temperature Boost (HTB) Power Processing Unit (PPU) Formulation Study

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Scope

This technical memorandum is to summarize the Formulation Study conducted during fiscal year 2012 on the High Temperature Boost (HTB) Power Processing Unit (PPU). The effort is authorized and supported by the Game Changing Technology Division, NASA Office of the Chief Technologist. NASA center participation during the formulation includes LaRC, KSC and JPL. The Formulation Study continues into fiscal year 2013.

A typical solar electric propulsion system for in-space propulsion includes solar arrays, a power management and distribution (PMAD) unit, a power processing (PPU) unit and a thruster, shown in Figure 1. The formulation study has focused on the power processing unit. The team has proposed a modular, power scalable, and new technology enabled High Temperature Boost (HTB) PPU, which has 5-10X improvement in PPU specific power/mass and over 30% in-space solar electric system mass saving.

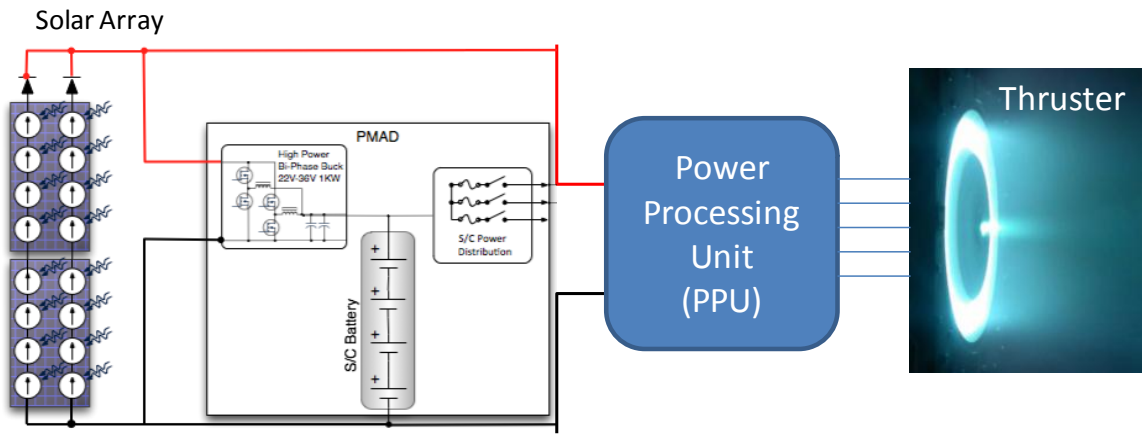

Figure 1. Solar electric propulsion system for in-space propulsion.

High Temperature Boost PPU

The High Temperature Boost (HTB) PPU has several new features, including a new system implementation, high temperature operation, non-isolated converter topology, and a new PPU architecture. It has been designed from the ground up to take advantage of emerging technologies, including both SiC technology and advanced high temperature packaging technology. Compared to the current state-of-the-art (SOA) PPU technology, the HTB PPU delivers a PPU capability with both high power and high specific impulse, while achieving low mass and high efficiency.

For a 320kW thruster-powered human exploration mission, the existing PPU technology would require 800kg PPU mass, while the HTB PPU would require only 91kg PPU mass. This is equivalent to an 88% mass saving at the PPU level, due to a 10X improvement in PPU specific power or specific mass.

Considering total power system mass, defined as the total mass of the solar array (such as ROSA), PMAD and cabling, radiator and PPU, the state-of-the-art PPU technology and the HTB PPU would result in 2869kg and 1976kg respectively for 320kW of thruster power.

This 30% mass saving at the power system level is a direct result of the radiator mass savings resulting from the HTB PPU being capable of operating at higher temperature.

In addition to the in-space mass saving, the HTB PPU is modular and provides power scalability from 10kW up to 80kW per PPU, a 2-16X increase in power at PPU level when compared with the current state of the art.

HTB PPU Proposed

Shown in Figure 2, the size of the HTB PPU is 12”x 4”x 8”. There are five slices or modules:

- 10kW Anode Discharge Power Module,
- Magnetic Supply Module,
- Cathode Supply Module,
- Control/Valve Drive/House Keeping Module, and
- Input/output Filter Module.

All modules are bolted mechanically and can be separated as five individual modules. A set of one each for the Magnetic Supply, Cathode Supply, Control/Valve Drive/House Keeping Supply, and Input/output Filter modules are designed to support up to eight of the 10kW Anode Discharge Power Supply modules, shown in the right lower corner in Figure 2.

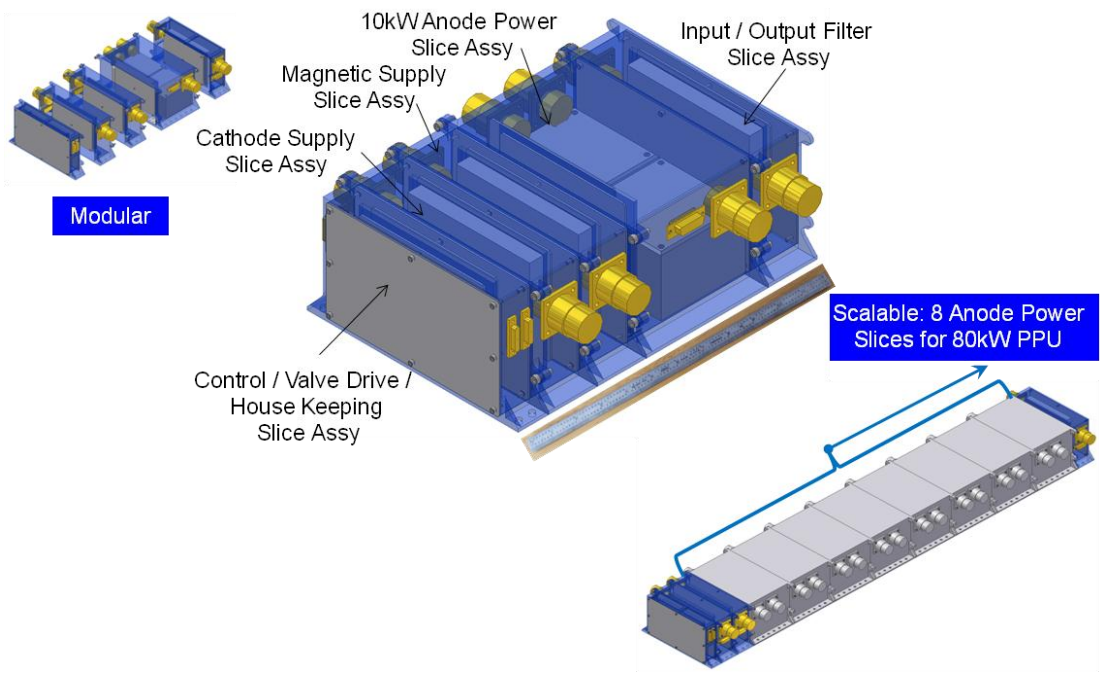

Figure 2. Modular and scalable HTB PPU: 10-80kW/PPU without redesign.

Figure 3 shows the HTB PPU in a SEP system with the solar array, PMAD, PPU, and a Hall thruster with a xenon feed system. Highlighted in the green boxes are the HTB PPU and its five modules.

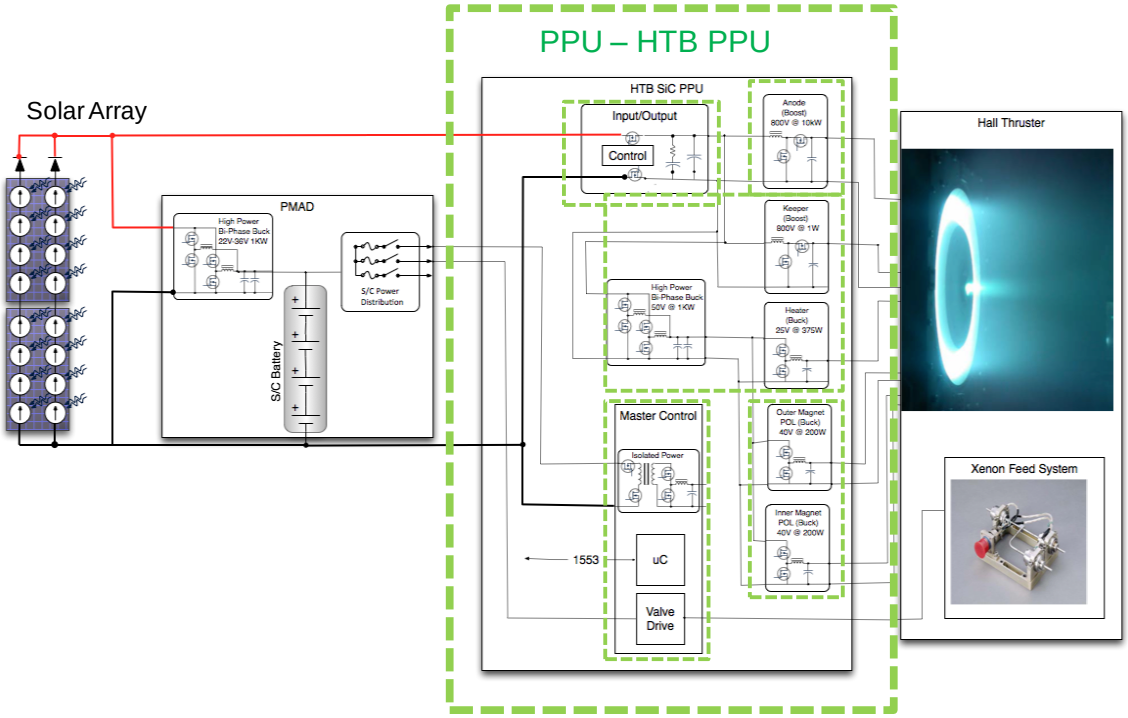

Figure 3. Solar electric propulsion system with HTB PPU and its five modules.

In summary, the proposed HTB PPU is modular and scalable from 10kW per PPU to 80kW per PPU, allowing it to provide 320kW thruster-power for a 4-thruster configuration without redesign.

Basic Concept of the HTB PPU

As outlined above, the basic concept of the HTB PPU is to increase power and efficiency, and to reduce PPU and system mass and volume by using 1) high temperature SiC device technology and high temperature packaging technology; 2) new power system implementation and new design to take advantage of the emerging high temperature technology; and 3) non-isolation architecture.

During the Formulation Study, an end-to-end system engineering approach was applied to the new design to extract the most value from the emerging high temperature semiconductor and packaging technologies, and to achieve high temperature operation with a non-isolated topology for high power and low specific mass.

1. High temperature operation with lowered switching loss at high frequency to reduce mass and volume with comparable or better efficiency is achieved, because a) lower switching loss of SiC technology allows switching frequency greater than 100kHz to reduce the magnetic mass, and b) lower thermal resistance by advanced packaging technology enables the increase of power dissipation capability. In addition, operation of the baseplate at 100°C leads to reductions in the radiator size and mass as well as the total power system mass.
2. A paradigm shifting, novel power conversion architecture in the form of a classic non-isolated boost conversion topology is selected due to its simplicity, with a reduced

component count, easier control scheme and ground up design capability, which takes full advantage of SiC's unique strengths.

System Engineering

The end-to-end system analysis of a high power solar electric propulsion vehicle identified several opportunities for improving the specific power (kW/kg). The lower specific power of the solar array drives the need for technology development in all areas to improve the overall efficiency and bring up the system level performance.

System Architecture

One area of improvement is in the system architecture. With the long-term goal of a 320 kW solar electric propulsion vehicle, the architecture must be scalable to reduce the risk for near-term technology demonstration missions. The architecture will also need to accommodate multiple lower-power thrusters to achieve the 320KW goal. Early systems might demonstrate multiple lower-power thrusters and then scale up as the Hall thrusters improves.

High power, four thruster solar electric propulsion architectures for the HTB PPU and the SOA PPU are compared in Figure 4. As shown in the plot, the scaled HTB PPU offers a mass savings for a wide power range over the SOA PPU, with significant savings at 320kW. A scalable PPU can power the lower-power thrusters and then scale up to the higher-power thrusters, without sacrificing the specific power performance or the early investment in PPU development, given in Figure 5.

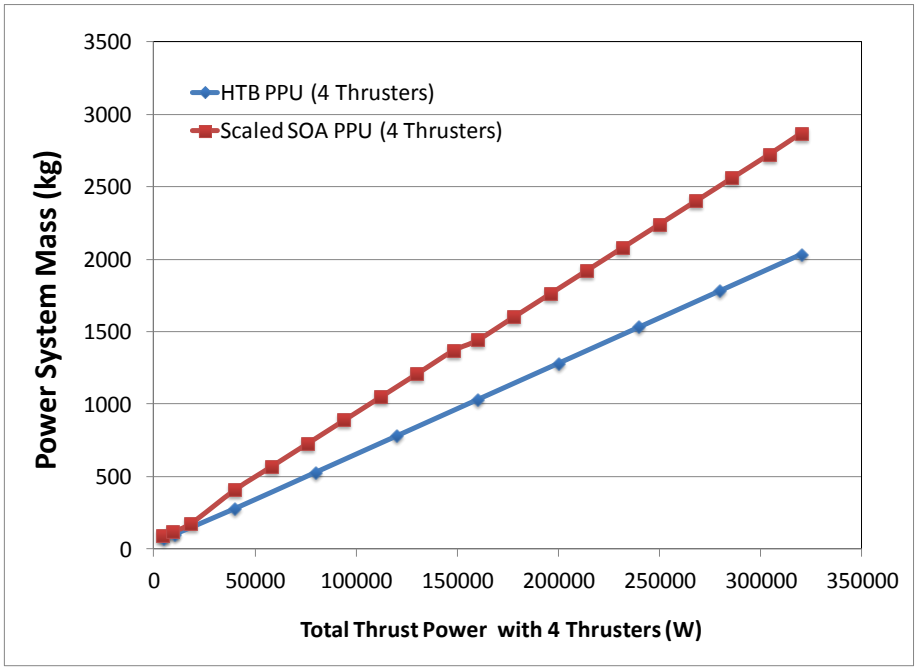

Figure 4. Total power system mass for four-thruster power configuration.

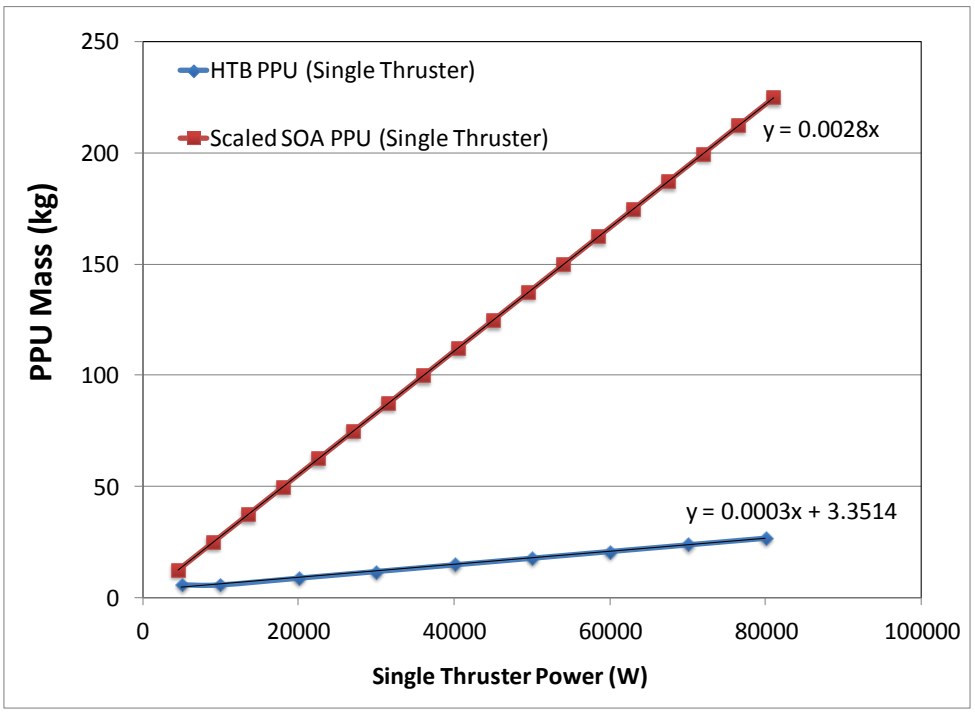

Figure 5. Scaling power for HTB PPU versus state-of-the-art PPU.

First, the system power bus voltage needs to increase to reduce the mass of the cabling and PMAD. The PPU runs off the higher bus voltage and increases the overall efficiency. In addition, a higher output voltage will enable the Hall thrusters to run at higher specific impulse, reducing the mass of the xenon to achieve the same amount of delta-V [1].

On the front end of the PPU, a local power switch on the high voltage power bus input is designed to reduce the need for a centralized high voltage power distribution, thereby reducing the impact of system scale up to high power. The PPU is designed to meet the higher voltage, and the input switch is sized for the PPU current level. For multiple thruster systems, the PPUs are added per thruster without the need of changing the scale of a centralized power distribution unit.

Second, the PPU efficiency is a key driver in the development of the PPU due to the impact on the overall system in size of the solar array and the size of the radiator to maintain the temperature of the electronics. The more efficient power converter topologies are non-isolated. The sensitivity of the power system mass to PPU efficiency is 21kg per 1% leading to 104 kg savings between the HTB PPU and SOA PPU at 320 kW total thruster power. As long as the system architecture can tolerate a Hall thruster connected to the single point ground of the power system, the overall system specific power will increase.

The size of the radiator for the PPU electronics is another factor in the system specific power. In addition to higher efficiency, a high operational temperature will reduce the size of the radiator. Current SOA PPUs have a maximum operating temperature of 50°C. A PPU with a baseplate operating temperature of 100°C will reduce the area and mass of the radiator by a factor of two. The parameters for the power system mass model are identified in Table 1.

Table 1. Power System Mass Model

SOA/TRL9 PPU	Efficiency 92% for Anode power, 90% for auxiliary Mass scaled at 2.8 kg/kW, One PPU per thruster Auxiliary load is 10% of Anode power
HTB PPU	Efficiency 96% for Anode Power, 90% for auxiliary Mass for single PPU is 2.8 kg + 0.25 kg/kW, One PPU per thruster Auxiliary load is 10% of Anode power
Solar Array	Mass 200 W/kg Voltage 200 V
PMAD	Spacecraft load 1 kW Mass 10kg
Cable	Distance 5m Mass 34g/m per conductor 6mohm/m per conductor, number of conductors to get 1% loss
Radiator	Mass 4.2 kg/m^2 100C, 1.5m^2/kW; 50C 3.4m^2/kW

Cathode Current Sharing

Two issues for the multiple-thruster configuration that need to be addressed are cathode current sharing for multiple thrusters and leakage current from the spacecraft plasma through micrometoriod holes in the cover of the solar array [2].

Figure 6 shows the different options for addressing the issue of cathode current sharing. The cathodes of the Hall thruster are connected to the power return of the PPU. In a non-isolated system, the Hall thruster and PPU power return are connected directly to the power system single point ground. In a multiple thruster configuration, the cathodes of each thruster are eventually connected together through the power system single point ground. The plasma created by the Hall thrusters enables the return current from each of the thrusters to return though the lowest impedance path to the power system single point ground. The cathodes do not force current sharing but instead exhibit behavior similar to a negative temperature coefficient, where impedance is reduced as current increases. Because of this effect, current from all of the thrusters flows through a single cathode. This results in an increase in cathode temperature and could impact the operating lifetime of the cathode.

The options for forcing the current to share in the cathodes are as follows:

1. Isolated PPU: Isolation forces the individual Hall thruster current to return through a designated cathode to the PPU power return. The PPU power return is isolated from the single point ground through galvanic isolation, preventing any cathode from carrying more current than one Hall thruster.

2. Resistor ballast sharing: A resistor between the PPU power return and power system point ground will force current sharing between cathodes due to the “I X R” delta V. The size of the resistor needs to compensate for the difference in impedance between the cathodes.

3. Segmented array: By dedicating portions of the solar array to individual Hall thrusters, the power system will have several single point grounds with impedance between each point to prevent ground loops.
4. Active current sharing: Current can also be forced to share by placing a transistor in the return path between the PPU and the power single point ground. This transistor can be operated in the linear mode, varying the impedance to force the current to share in a way that is similar to the ballast resistor approach. This approach can accommodate a larger difference in impedance between cathodes.

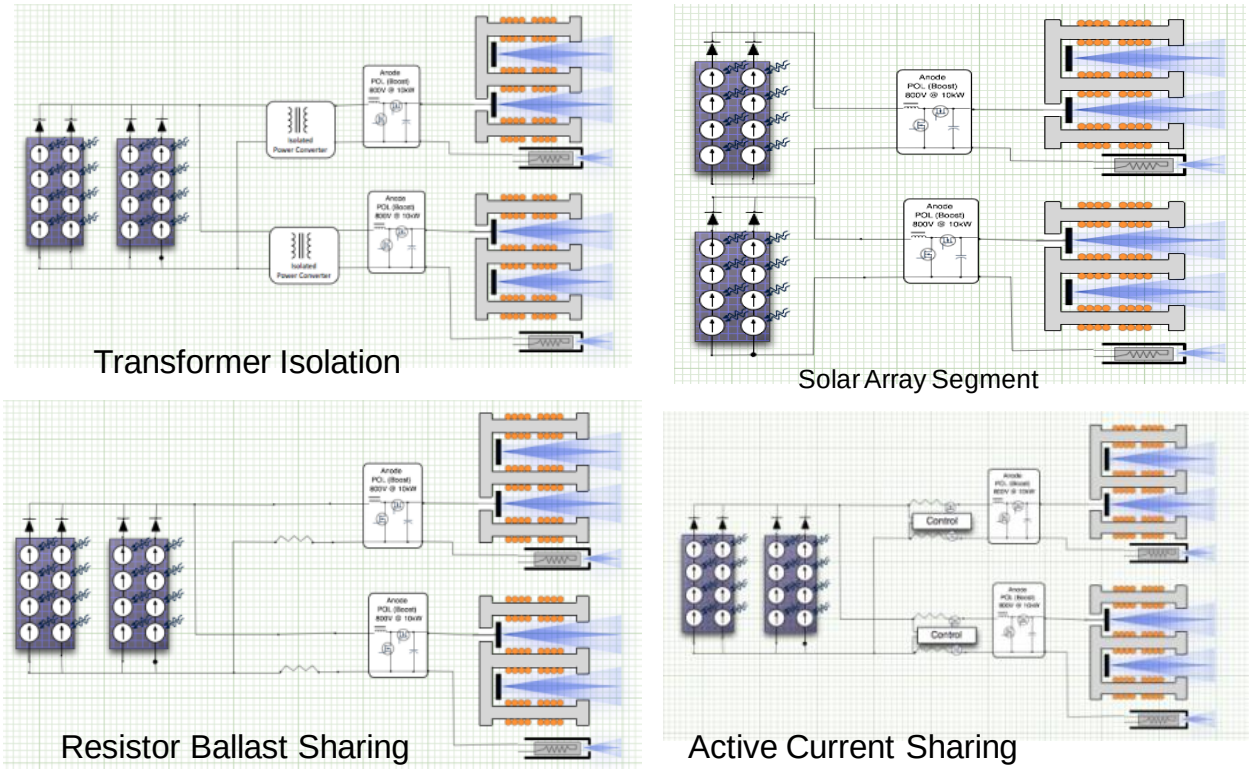

Figure 6. Cathode current sharing options.

Early testing has indicated that a current sharing resistor can balance the cathode current, and the size of the hole in the solar array will limit the leakage current. The impact of the power loss in the current steering resistors and loss due to leakage needs to be covered by the improvement in efficiency. Part of the future work includes an assessment of the power loss for these two factors as compared to the improvement in efficiency to support the non-isolated topology selection.

Converter Topology

The converter topology selection trade has considered efficiency and power density as its highest valued performance parameters. Further, consideration has been given to topologies that would make the most of new advances in power semiconductor devices.

The following section will first delve into the conventional approach to topology selection when using Si based parts. From there we highlight how this conventional paradigm does not yield the most effective solution when SiC parts are employed.

And finally, the section wraps up with a summary of what the topology selection gains over the conventional state of the art when the proposed topology selection is coupled with a design operating point that is tailor matched to the high temperature SiC devices proposed.

Conventional Approach

Traditionally, the conventional conversion topology is the full bridge for this power level [3-4]. This paradigm is so fundamentally accepted, it is no wonder that many miss that the trade to the full bridge presupposes the use of Si parts and the constraints these parts bring to the topology selection discussion.

Most often, this topology is required to achieve conversion ratio, isolation, and/or reduce primary switch stress [5-6]. Operating point (selected switching frequency, duty ratio, conduction mode) and design values (inductance/capacitance values, device choice, etc.) are selected around widely accepted constraints related to:

1. Need to stack secondary, easy primary switch stress, greater power handling capability, or hard requirements for galvanic isolation.
2. The thermal characteristics of commercial device packaging.
3. Conventional prioritization of performance parameters often focuses on output ripple, transient response, wide conversion range (for wide input), and would often put efficiency and heat generation far above weight and/or volume.

Converter Topology in HTB PPU

Conventional wisdom on topology and operating point does not capitalize fully on the availability of new devices nor does it fully consider the differences in the space application. With SiC MOSFETs in production and more feasible, we have devices with higher junction temperature tolerance, higher breakdown voltage, and lower switching loss. These improvements effectively change the 'trade space' and present a new conclusion to a design trade that had long since settled on the full bridge for this power level.

First, the lowered switching loss means we can operate with a higher switching frequency, resulting in drastically reduced magnetic mass. When coupled with thermal mass, the magnetic mass makes up the largest portion of the converter mass fraction. Second, the higher junction temperature tolerance means we can operate with less hear rejection mass in the converter as well as throughout the system. These two advantages alone make for game changing improvements in the power density area.

In addition, higher breakdown voltage than a Si part with comparable on-state resistance means stacked secondaries may not be necessary in the high voltage supply.

And finally, the new materials may offer higher tolerance to the radiation environment.

As such, our team would like to offer a different perspective in which we propose a non-isolated bi-phase, hard-switched boost (shown in Figure 9), since it is the simplest approach, with the potential to be the most power dense and most reliable.

SiC MOSFETs have lower switching loss, higher junction temperature tolerance, and high voltage rating as compared to Si switches with comparable on state resistance. The combination of improved device performance, lower thermal resistance packaging, and current sharing scheme allow for a different, more power dense approach. In addition, stage interleaving reduces ripple and distributes heat load.

With increased breakdown voltage, stacked secondary stages are unnecessary and the conversion ratio we propose is within the capability of the boost. Regarding isolation, if direct drive is a manageable option then non-isolation is also manageable. In terms of operating point, we can use our junction temperature margin to increase the power density for applications that value power density.

Based on our analysis, we can combine improvements in device materials/physics (increase junction temp tolerance, lower switching losses) with improvements in junction to case thermal resistance to work all sides of the equation.

We will use the margin by increasing switching frequency (means smaller/lighter magnetics, reducing thermal mass, and allowing for higher base plate temperature).

Trade Study

Based on the Cree datasheet information for comparable MOSFETs, we apply this data for R_{th}, switching and conduction loss for the MOSFETs as well as diode model parameters for the freewheeling diodes in order to develop a baseline for SiC performance. For the purposes of the trade study, we use this data, shown in Table 2, for comparative purposes only in down-selecting our target topology.

Table 2. Switching Loss and Thermal Resistance Data used in Temperature rise and Efficiency Loss Calculations

Junction Temperature (C)	R_{th}, Junction to Case (C/W)	R_{cs}, Case to Sink (C/W)	CREE Data E_{swon} (μJ/pulse)	CREE Data E_{swoff} (μJ/pulse)	CREE Data R_{dson} (Ohms)	CREE Data Diode Model VT (V)	CREE Data Diode Model RT (Ohms)
125	0.58	0.25	422	329	0.095	0.795	0.056875
25			530	320	0.08		

In total, the team considered seven combinations of topology, design operating point, and module size. These included (1) 10kW hard-switched boost, (2) 5kW hard-switched boost, (1) 10kW hard-switched boost (aggressive), (1) 10kW soft-switched boost, (2) 5kW soft-switched boost, (1) 10kW full bridge and (2) 5kW full bridge.

In general, preliminary calculations showed that the boost had the potential to have less mass as the isolation transformer of the full bridge is considered. Since the team was pursuing non-isolated options for the converter, the only other reasons to go with full bridge (i.e., conversion ratio and lowed device stress) were somewhat less compelling for our target application. SiC has a higher voltage rating, for a comparable on state resistance,

and lower switching losses than a comparable device in Si. Operating the variable output voltage at 800V would effectively be the end of the line for the boost's conversion range. Although it is doable operating at this duty cycle results in a more difficult control problem. Ultimately, the full bridge was ruled out based on these considerations, the part count comparisons, as well as preliminary loss and mass predictions.

Within the boost options, we recognized that the boost is not traditionally employed at these power levels. As mentioned above, the reasons for this largely revolve around device capabilities and not the fundamental topology limitations, beyond isolation. Traditionally, lowering switching losses in the main switching elements is a tactic used in advanced power stages to further converter capacity by lowering device stress at a particular power level. One can see in Figure 7 and Figure 8 below that the nonzero overlap of the drain to source voltage across the switch while current ramps up through the switch resulting in a non-zero switching loss during the on and off transition.

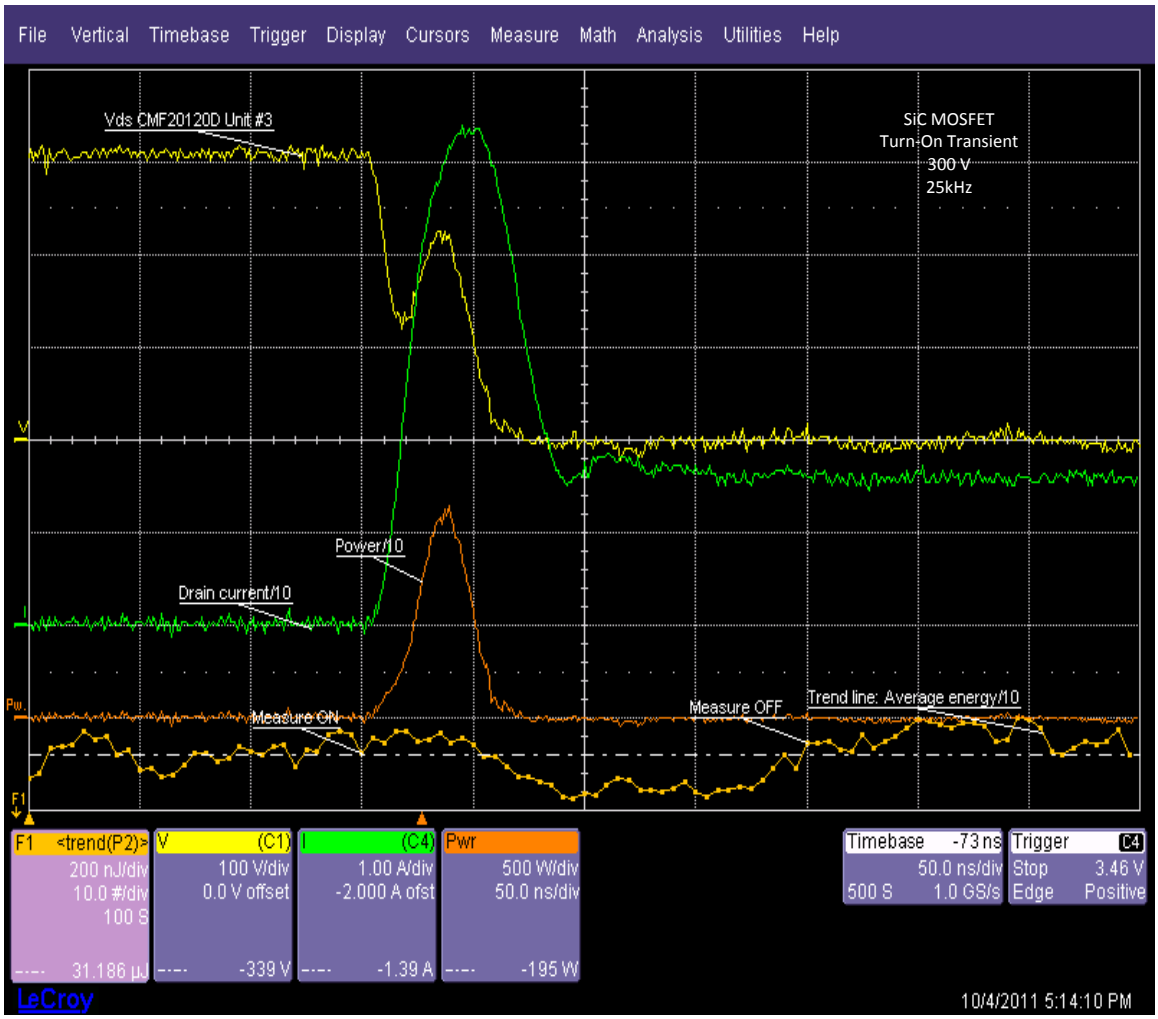

Figure 7. Scope capture of SiC MOSFET turn on transient at 300V and 25kHz.

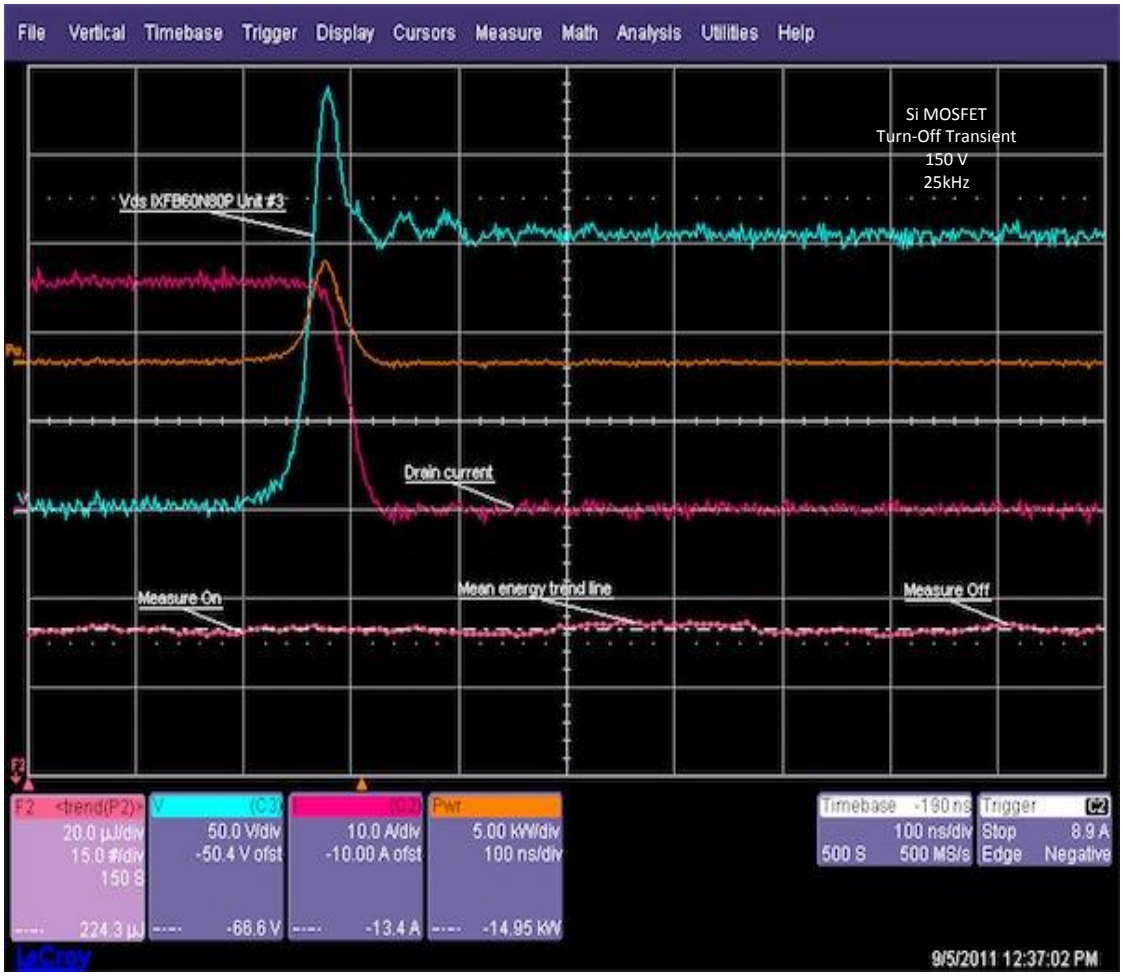

Figure 8. Scope capture of SiC MOSFET turn-off transient at 150V and 25kHz.

Soft-switching converters employ additional reactive components to form resonant circuits in one or more modes of circuit operation that work to resonantly drive voltage or current to zero before switch transition thus reducing the switching loss. However, since SiC already has lowered switching loss as compared to Si, the team expected the benefits of soft-switching would have a diminished return when one considers the number of additional components and added complexity the soft-switch boost variant brings. In order to make this trade, the team did a first order converter design on two topologies, one hard switched (Figure 9) and one soft-switched (Figure 10) [7].

In Table 3, two key columns comparing hard to soft-switched topologies are shown. The trade study included loss predictions and showed the soft switching boost doubler as the lowest loss and highest power density. However, this topology was not selected due to its added complexity.

In the end, the simplicity of the hard-switched boost coupled with its good performance when compared to a soft-switched variety was selected at the target topology. The choice of (2) parallel 5kW modules to make up the 10kW capacity was based the desire to distribute of heat across the device case to sink area.

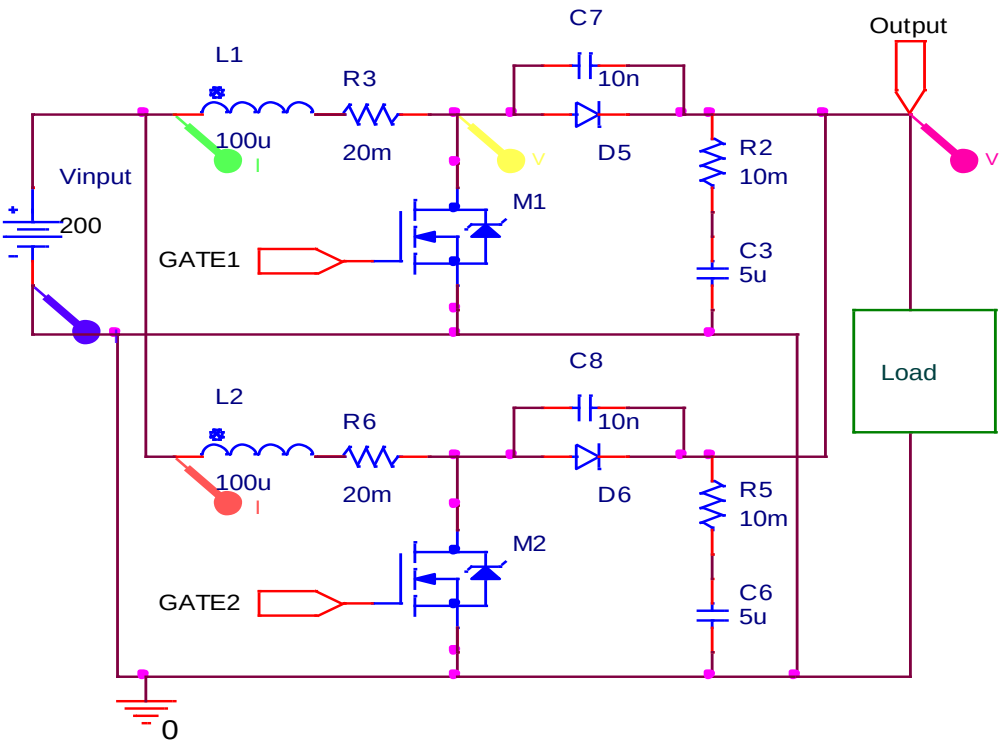

Figure 9. Bi-phase, hard-switched boost topology.

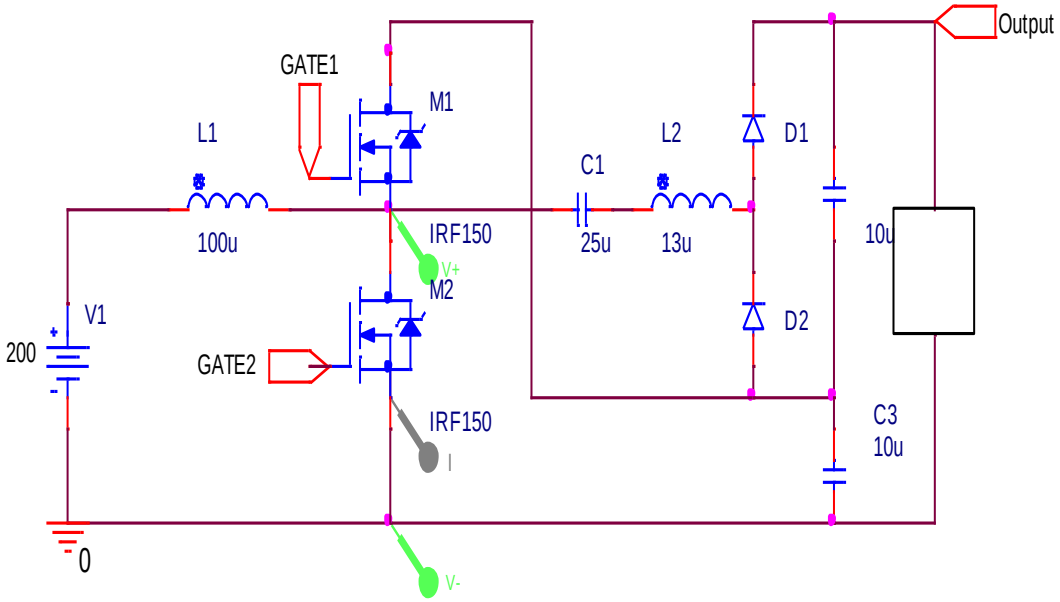

Figure 10. Boost with soft-switching.

Table 3. Excerpt from Topology Trade Study

	(2) 5kW Hard-switched Boost	(2) 5kW Soft-switched Boost
Operating Point Targeted by Analysis		
Input Voltage (V)	200	200
Output Voltage (V)	800	800
Switching Frequency (kHz)	100	100
Heat Sink Temp Hold to Temp (Degrees C)	100	100
Main Inductor Allowable Temp Rise (Degrees C)	80	
Average Input Current (per module-Eff. 90%) (2)	27.8	27.8
Main Inductor Value (uH)	200.0	100.0
Inductor Operating Mode (CCM or DCM)	CCM	CCM
Output Capacitor Value	5.0	5.0
Total Load 10kW Across X Modules (# of units)	2	2
Quantative Measures		
Output Ripple (Delta Vo/Voavg)	0.4%	3.0%
Capacitor Current (RMS)	6.35	7
Delta iL ((iLpeak-iLmin)/iLavg)	29.9%	45.7%
Qualititative Measures		
Isolation	No	No
Conversion Range	Fair	Good
Control Complexity (1,2)	Moderate	Moderate
Control Difficulty (1,2)	Moderate	Moderate
Devices and Device Stress		
Main Switch Stress (V)	800	476
Main Switch Stress (I in Amps pk/RMS/Avg)	29.4/22.5/19.8	51/26/18.5
Main Switch Stress (I in Amps pk)	29.4	51
Main Switch Stress (I in Amps RMS)	22.5	26
Main Switch Stress (I in Amps Avg)	19.8	18.5
Aux Switch Stress (V)	N/A	
Aux Switch Stress (I in Amps)	N/A	
Diode Stress (V)	800	325
Diode Stress (I in Amps pk/RMS/Avg)	29.4/11.9/5.6	26/10.4/6
Diode Stress (pk)	29.4	26
Diode Stress (RMS)	11.9	10.4
Diode Stress (Avg)	5.6	6
Number of Switches	2	4
Number of Diodes (1)	2	4
Number of Inductors	2	4
Number of Capacitors	2	6
Number of Transformers	0	0
Losses		
Main Switch Conduction Losses (Total in W)(1,2)	96	128
Main Switch Switching Losses	181	120
Aux Switch Conduction Losses (Total in W)(1,2)	N/A	
Aux Switch Switching Losses	N/A	
Diode Conduction Losses (Total in W)(1,2)	26	20.5712
Diode Reverse Recovery Losses	5	0
Main Inductor Core and Copper Losses (W)	60	
Capacitor (Total in W)	8	
Copper Losses (Total in W)	30	
Total Losses	376	
Temperature		
Main Switch Junction to Sink Rth (C/W)	0.83	0.83
Main Switch Junction Temp (C)	**215**	**203**
Main Inductor Core Temp (C) (6)	179	
Mass		
Main Inductor (g)	906	
Aux Inductor (g)	N/A	
Capacitor Mass (g)	700	
Semiconductor Mass (g)	24	
Buss and Cable (g)	500	
Enclosure/Heat sink (g)	2000	
Total Mass (kg)	3.43	
alpha (kg/kW)	**0.343**	
Efficiency	**96.2%**	

System and Device Packaging for HTB PPU

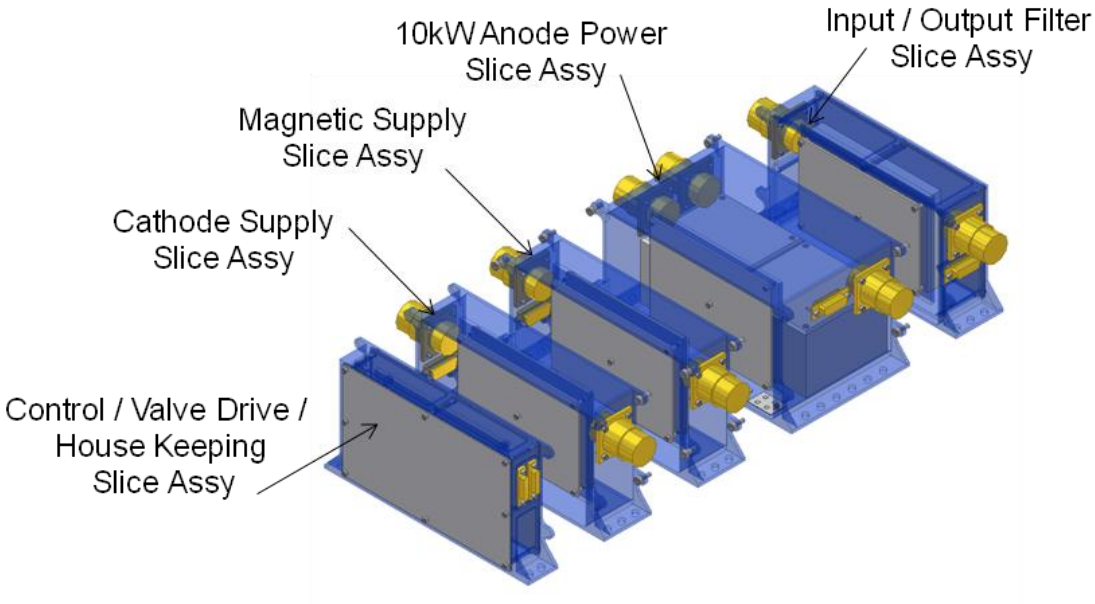

Figure 11. HTB PPU slices/modules.

High Temperature Slices/Modules

The system packaging architecture for the HTB PPU was designed around the idea of modularity, scale-ability, flexible integration, flexible test scenarios and re-workability to reduce spacecraft volume and mass. The configuration implements a packaging baseline architecture made up of 5 horizontally mounted aluminum slices that are 208.7mm (8.2in) x 110.0mm (4.3in). Slice to slice and slice to radiator retention are bolted interfaces. The design becomes scalable by adding any number of particular slice functions as noted in Figure 2 and Figure 11. In reverse, slice removal is accomplished by removing its associated bolted interface on both adjacent slices. Because of this simplified method, only the associated slice is influenced by disassembly rather than the entire module

With the slices mounted in a horizontal configuration each slice provides its own dynamic and thermal paths. The machined web and mounting feet provide the unidirectional conduction path for each slice. Heat from the Printed Wire Board Assembly (PWBA) or individual web mounted components can maintain desired or allowable components junction temperatures with the base plate temperature of 100°C.

Since component packaging technologies play a significant role in our modular solution, Figure 12 and Figure 13 show the simulated thermal gradients for the 10KW Anode Slice, comparing the difference between a Chip-On-Board (COB) package solution and a standard TO-247 package.

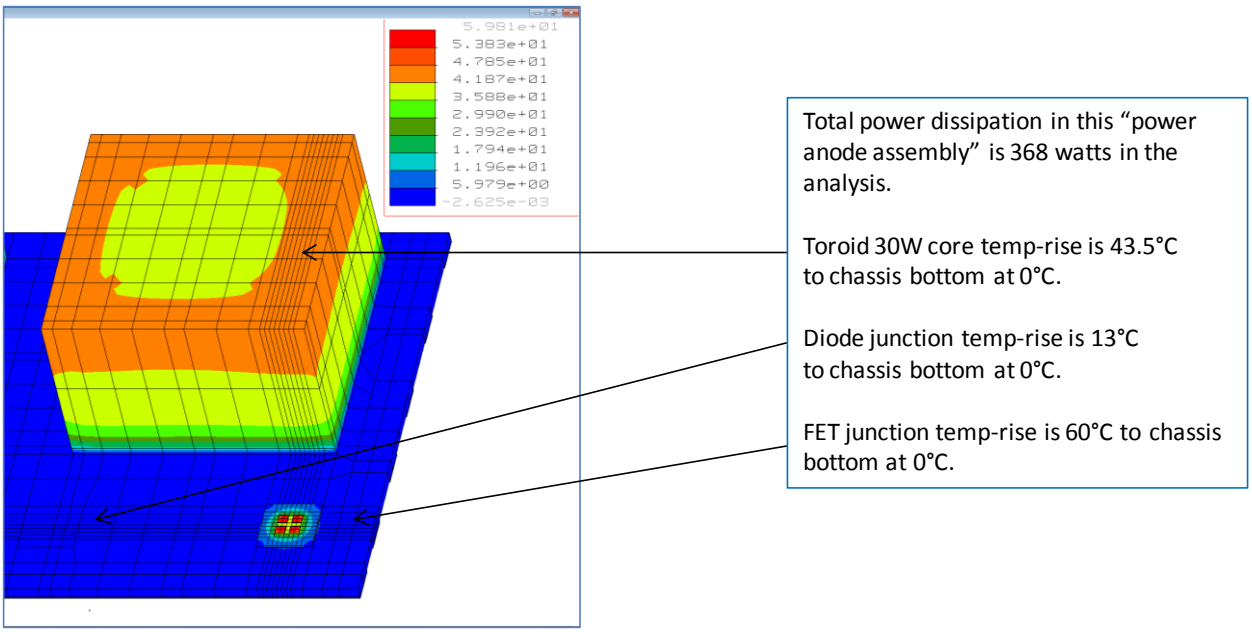

Figure 12. Thermal profile of the 10kW anode discharge supply assembly for with SiC MOSFET in COB package.

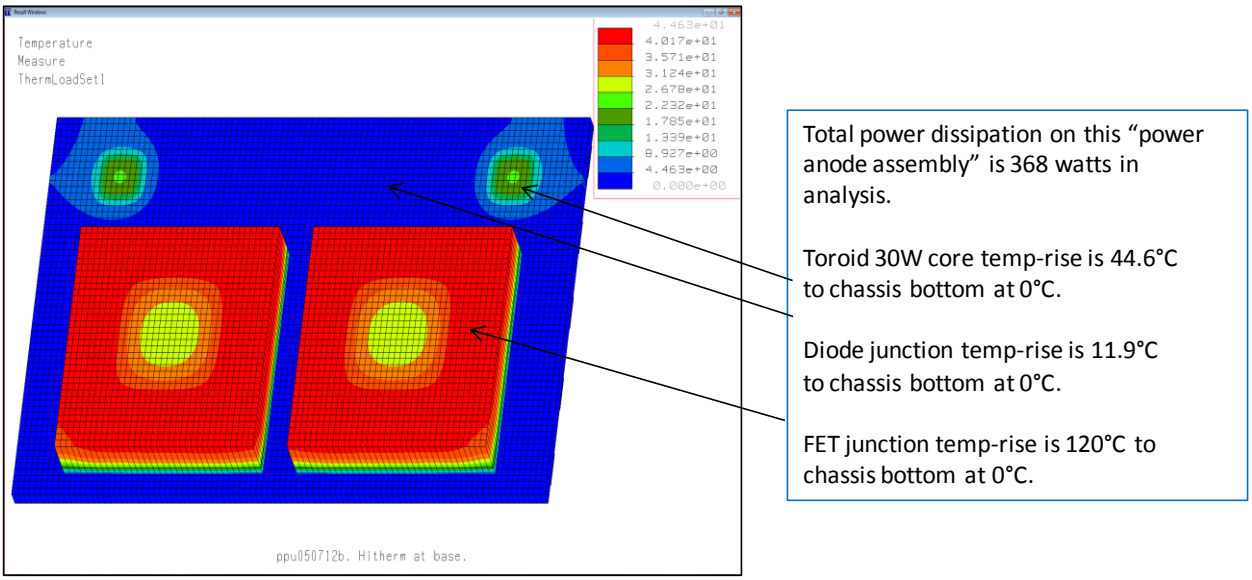

Figure 13. Thermal profile 10kW anode power supply assembly with standard SiC MOSFET T0-247 package.

I/O's between slice to slice and thruster interfaces will be handled using extreme environment connectors capable of carrying 80A @ 180°C.

A baseline mass summary for the individual modules is shown in Table 4.

Table 4. Slice/Module Mass Summary

Slice Assy Mass	Propose	Target
Input / Output Filter	1.0Kg	1.0Kg
10kW Boost Power	3.0Kg	2.5Kg
Magnetic Supply	1.2Kg	0.5Kg
Cathode / Heater Supply	2.0Kg	0.5Kg
Ctrl / Buck Pwr / Valve Drive	2.0Kg	0.8Kg
Total:	9.2Kg	5.3Kg

Packaging technologies for each slice/module were selected based on the expected maximum junction temperature, as well as the maximum current, maximum voltage and complexity (number of components and layers of circuitry). These requirements are summarized for each module in Table 5.

Table 5. Slice/Module Requirements Summary

Slice/Board	Temp (°C)	Current (A)	Voltage (V)	Complexity (Parts/ Layers)	Size (cm x cm)	Cycle (°C)
I/O Filter	160	50	800	10uF capacitors	Cap size	160 to -15
10kW Anode Power Supply						
Power	220/160	50	800	1-2 layer	2.54 x 2.54	220/160 to -15
PWM Control Board	160	0.18	28	8 layer	17.78 x 10.16	160 to -15
Magnetic Supply	160	20	200 (in)	8 layer	17.78 x 10.16	160 to -15
Cathode/Heater						
Cathode Keeper	160	0.125	800	8 layer (30 components)	17.78 x 10.16	160 to -15
Cathode Heater	160	5	100			
Ctrl/Buck Power/Valve Drive	160	2	28	12 layer (200 components)	17.78 x 10.16	160 to -15

Packaging Technologies

Materials selected for use in high temperature electronic packaging applications must be capable of withstanding extended operation within the target environment. Therefore, a clear understanding of the mechanisms that dominate immediate and time dependent failures in this regime must be understood to maximize reliability. Failures that occur immediately upon exposure to high temperatures include plastic deformation, melting of materials, and change in resistance or capacitance with increasing temperature. This will influence the selection of substrate materials, since several polymers are no longer effective for use at the target temperatures, and passive devices. Processes that occur over many cycles or after extended exposure to the target operating conditions include fatigue, creep, diffusion, oxidation, changes in resistance or capacitance with time at temperature, and electromigration. Coefficient of thermal expansion (CTE) differences between the die and the substrates are major sources for stresses within these assemblies, as well as that between the heavy current carry conductors and the substrate. In addition, phase and microstructural changes combined with diffusion and oxidation influence the strength, ductility and conductivity of the different materials. Die pads, wire, substrate plating and substrate conductor materials must be carefully selected to minimize diffusion and the formation of secondary phases as well as voids at interfaces, such as those observed with Au wirebonds on Al bondpads at temperatures greater than 150°C. Finally, all of these issues combined with the applied current can yield electromigration problems. The correct selection of materials for electronic packaging can help minimize several of these issues.

High Temperature Device Packaging

The substrate and board technologies were separated based upon the current and complexity requirements. Both the Anode Power Supply Board and the I/O Filter require currents of up to 50A, with very low complexity requirements of 1-2 layers. To meet the high current and heat dissipation requirements, Direct Bond Cu (DBC) on Al_2O_3, DBC on AlN, or Si_3N_4 Active Metal Bonding (AMB) are selected. Each of these substrate types offers thick Cu conductors on relatively high thermal conductivity substrates. The thermal and mechanical behaviors of the three substrates are summarized in Table 6. Each of the substrate technologies discussed is compatible with thick Cu traces. Depending upon the number of thermal cycles required, reliability of the substrates may become a problem. Si_3N_4 has exhibited higher thermal cycle reliability due to its higher strength.

Table 6. Comparison of Ceramic Substrate Materials

Material	Dielectric Constant	Thermal Conductivity (W/m·K)	Flexural Strength (MPa)	Coefficient of Thermal Expansion (ppm/K)
Al_2O_3 96%	9.5	26	400	7.4-8.2
AlN	8.6-10.0	140-220	207-345	4.3-4.6
Si_3N_4 (SN460)	8	58	850	2.7

The remainder of the boards require significantly lower currents of <5A, with the exception of the Magnetic Supply which requires 20A for select portions of the circuit. In addition, these boards require significantly greater complexity (8-12 layers and up to 200 components). For these modules, the following substrates will be considered: high temperature polyimide circuit boards (IPC 4101/41), high temperature co-fired ceramic (HTCC) and low temperature co-fired ceramic (LTCC). A comparison of these board materials is shown in Table 7.

Table 7. Comparison of High Temperature Multilayer Circuit Materials

Material	Primary phase	Thermal Expansion (ppm/°C)	Dielectric constant	Dielectric loss	Thermal conductivity (W/m-K)	Flexural strength (MPa)	Density (g/cc)
HTCC	Al_2O_3	7.1	9.5	0.0004	25	420	3.9
	ALN	4.4	8.9	0.0004	175	320	3.3
	SiC	3.7	45		270	441	
LTCC	Glass-matrix, crystallized	3–7	3.9–7.5	0.0002–0.003	2	180–210	2.25–3.0
HT PCB	E-glass/ Polyimide (Tg=220-300C)	11-14 x,y 60-80 z	4.5 z		0.35		

As stated previously, the materials for bond wires and substrate metallizations must be carefully selected to avoid the formation of detrimental secondary phases and voids at the bond. A summary of the high temperature limits of various wire/bond pad combinations is provided in Table 8.

Based on these limitations, the substrates used for this project will be Ni plated with a thin Au layer for oxidation resistance. Au bond wires will be used for devices with Au top metal and Al bond wires will be used for devices with Al top metal.

Table 8. Maximum Use Temperature for Various Wire and Bond Pad Combinations

Wire/ bond	Max T (C)	Reason
Al-Au	175	Forms brittle intermetallics which reduce bond strength and conductivity.
Cu-Al	200	Forms brittle CuAl2 intermetallic phases that lower shear strength.
Cu-Au	300	Interdiffusion creates excessive voids that decrease the bond area and strength.
Al-Ni	300	Interdiffusion creates excessive voids that decrease the bond area and strength.
Al-Al	660	Melting temperature.
Au-Au	1064	Melting temperature.

Device and component attachment materials selection is dominated by the high temperature mechanical strength, CTE and thermal conductivity of the material. A summary of these properties for several potential attachment materials is provided in Table 9. To minimize stresses within the device, die attach materials should be selected with a melting temperature that is well above the use temperature but not so high that the device degrades during processing. In addition to die attach, these materials will be used to attach passive devices and possibly select packaged devices to the substrate or printed circuit assembly. Attachment materials to be evaluated for this project include Au80Sn20, Sn5Pb95, ME8863.

Table 9. Property Summary for Various Attachment Materials

Material	**Melting Temp (°C)**	**Limiting Properties**	**Tensile Strength (MPa)**	**Elastic Modulus (GPa)**	**Thermal Cond. (W/m-K)**	**CTE (ppm/K)**
Solders						
Sn63Pb37	183	Eutectic MP	35.4-42.2	14.9	50	24.7
Au80Sn20	280	Eutectic MP	198	69	251	16
Sn5Pb95	308	Solidus	23.2	23.5	35	28.7
Au88Ge12	356	Eutectic MP	233	63	44	13
Au97Si3	363	Eutectic MP	255-304	69.5	293	11
Conductive Polymers	Cont. Use Temp (°C)					
ME8863	300	Chemical Degradation	Lap shear 6.9 MPa		1.0	30

Modular Packaging Details

10kW Anode Discharge Supply Slice represents the greatest challenge with respect to heat dissipation. A preliminary trade study was performed to determine the impact of chip on board (COB) packaging for the high power SiC MOSFETs. The COB solution assumed 80Au20Sn die attach and a direct bond Cu on AlN substrate. The single packaged high power device and the quad-MOSFET COB solution resulted in respective temperature rises of 120°C and 60°C. Both solutions assumed 138.5 W of dissipated power, 17.78mm x 17.78mm footprint, all bolted interfaces with a high thermal conductivity graphite interface

material, and temperature rises with respect to the chassis base temperature of 100°C. Based on this study, a COB solution was assumed. Since there are potential issues regarding cracking of the ceramic substrate during thermal cycling due to the presence of thick copper, the three substrate materials discussed above will be considered.

Input/Output Filter Slice consists of the 10μF, 800V, 200°C capacitors and required mounting boards. This supply is the least complex, electrically. The critical challenges associated with this slice are maintaining the mechanical integrity and electrical functionality of the large ceramic high temperature capacitor(s).

Magnet Supply Slice is a moderately complex module, which requires an 8 layer board and an array of inductors. The maximum current and voltage are 20A and 200V. To minimize the size and mass of this supply, we will explore the use of planar magnetics, which may be feasible due to the relatively low power. High temperature printed circuit boards as well as high temperature and low temperature cofired ceramics will be explored as potential substrate materials.

Cathode Supply Slice is a moderately complex board (8 layers) with a maximum voltage of 800 V and a maximum current of 5A. Board technologies under consideration include high temperature printed circuit boards, high temperature co-fired ceramic and low temperature co-fired ceramic.

Control/Valve Drive/House Keeping Slice is the most complex of the 5 modules, with 200 components and a 12 layer board. The maximum temperature is 160°C, with 2 A and 28 V. Although the operating conditions for this module are the least challenging, the increased complexity may result in assembly challenges and failure points. High temperature PCBs, high temperature co-fired ceramic and low temperature co-fired ceramic substrates will be considered.

Passives for HTB PPU

Availability of passive components designed or specified for use at high temperatures is generally limited. The behaviour of passive devices at elevated temperatures can be influenced by materials and design: however, suitability often depends on the required characteristics as a function of temperature and time. When high temperatures are coupled with high voltages for capacitors and high currents for inductors, the number of available long-life, high-value devices is further limited. In addition, significant derating of survivable components may result from power dissipation, current, voltage and operating life requirements, due to an increase in loss and a reduction in thermal conductivity. The resulting increase in internal temperature could destroy or reduce the lifetime of the devices. Finally, packaging and material degradation issues such as those discussed above (degradation of plastic encapsulants/adhesives, melting of solders, fatigue and overstress failure of leads) could result in variation of device behaviour and possibly failure if the passive component is not properly designed [8-9].

Capacitors

As mentioned previously, various parameters must be considered when selecting a device and significant derating often needs to be applied to compensate for reduced performance

during elevated temperature operation. For example, tantalum capacitors exhibit diffusion of the oxide layer into the tantalum electrode resulting in a reduction in the thickness of the dielectric with a concomitant reduction in the breakdown voltage of the dielectric, which can result in thermal runaway and catastrophic failure of the capacitor during elevated temperature operation. Additionally, large, brittle capacitors may fracture during thermal cycling due to the CTE mismatch between the device and the substrate. Such stresses must be taken into account during the device design. A summary of the published high temperature characteristics of various capacitor systems is provided in Table 10 [8].

Table 10. Typical High Temperature Behavior for Various Types of Capacitors

Type	Capacitance (C)	Dissipation (DF)	Temp. Ranges (°C)
Polymer			
(Kapton, Teflon)	Slight decrease	No change or slight increase	Max≈200-250 Data to 200
Ceramic, low/med-K	Small, variable changes	Large steady increase	Max 300-500 Commercial to 260 Data to 500
Ceramic, high-K	Usually a large steady decrease	Varies	Max 300-500 Commercial to 260 Data to 500
Thick film ceramic,K≈10	Varies, medium increase to ≈200°C, then rapid increase	Varies, small change to ≈200°C, then rapid increase	Max 250-300, Maybe 500 Some data to 500
Porcelain	Medium steady increase	Approximately constant	Max 300 Data to 300
Glass	Medium steady increase	Large steady increase	Max ≈300? Commercial to 200 Data to 450
Glass-K	Large steady decrease	Variable behavior, higher than glass near RT, may be lower than glass at HT	Max≈300? Commercial to 200 Data to 450
Electrolytic (solid dielectric	Relatively large steady increase; Al somewhat less increase than Ta	High, slight increase; Al lower than that of Ta	Max≈200-250 Commercial to 200 Data to 300
Mica, mica paper	Small increase or decrease to 200°C, variable above 200°C	Medium steady increase	Max≈300-500 Commercial to 300 Data to 300 (480)
"Simple" ceramics: alumina, beryllia, PBN	Medium steady increase to very high temperatures	Medium steady increase	Max to 600 Data to 600

While some capacitors, which are stable at elevated temperatures, are commercially available, they are often made of insulating materials with low dielectric constants and therefore have low energy densities. Table 11 [10] provides dielectric constants for various materials of interest for high temperature capacitors. Capacitance and dissipation factor for several ceramic capacitors as a function of temperature to 500°C are provided in Figure 14. Commercially available capacitors made with higher dielectric constant insulators tend to exhibit unstable capacitance and high leakage currents at elevated temperatures. As seen in the Figure 15 plot [10], high dielectric constant ceramic capacitors based on barium titanate formulations exhibit variations in dielectric constant and dissipation factor with temperature. Those that exhibit stability, such as NP0, have a low dielectric constant in the region of interest. Although there are methods of self-healing that have been applied to various capacitors, such as thin metalized polymer film capacitors and tantalum electrolytic capacitors, these methods can only slightly improve the high temperature, high voltage performance of these devices. Therefore, the more stable low dielectric constant materials were selected. However, due to the low dielectric

constant and significant derating required, the devices selected are quite large. Three companies capable of providing adequately sized and mechanically robust NP0 capacitors were identified. One additional company provided two different high temperature mica solutions.

Table 11. Dielectric Constants for Various Materials

Material	Dielectric Constant
Air	1.004
Most polymers	2-6
Highest polymers	16
Most ceramics	4-12
Al_2O_3	9
Ta_2O_5	25
TiO_2	90
$BaTiO_3$	1500
SiO_x	3.9
Ceramic formulation based	20-15,000

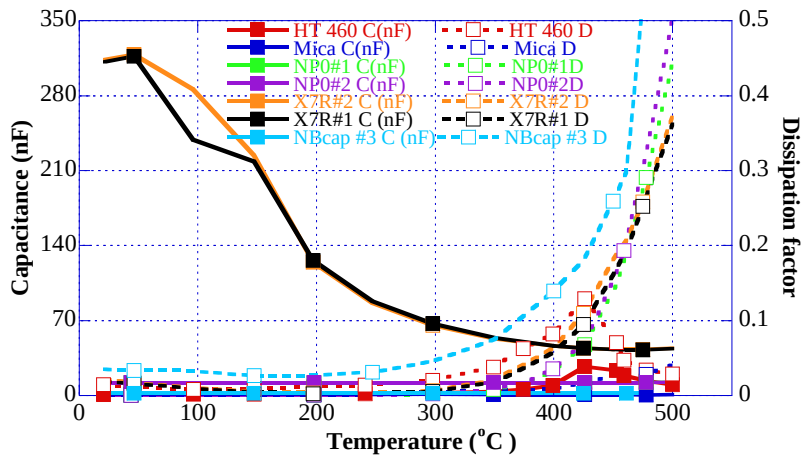

Figure 14. Capacitance and dissipation factor as a function of temperature for various high temperature capacitors.

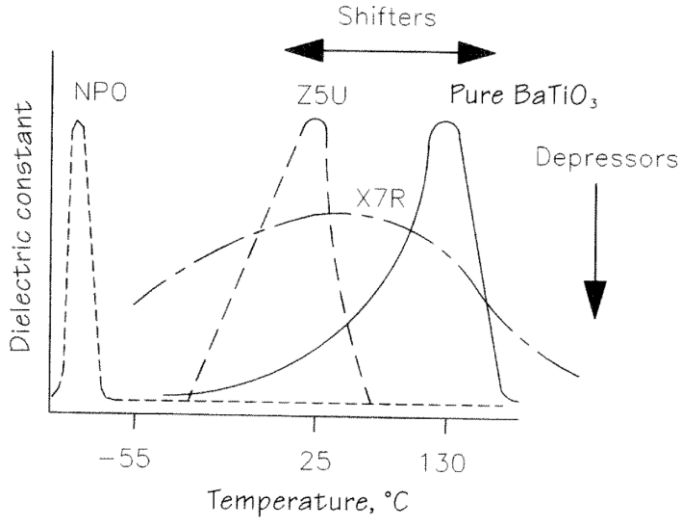

Figure 15. Temperature dependence of dielectric constant for pure barium titanate and various related formulations.

Inductors

For high temperature inductors, as with the previously discussed passive devices, performance and survivability at elevated temperatures is dependent upon the choice of materials, including the magnetic core material as well as the conductive and insulating materials for the windings. It should be noted once again that the maximum temperature expected for the high temperature inductors is 160°C. Standard transformer technologies are usable to 200°C [8]. To minimize the size and mass of this supply, we will explore the use of planar magnetics, which may be feasible due to the relatively low power. We explored the use of planar magnetics for the Boost Power slice, but the required flux density of the core exceeded that achievable using this technology. Fine powder cores based on MPP (Mo-Ni-Fe) and Sendust (Al-Si-Fe) will be considered and Cu wires with high temperature polymer insulation. If the temperature requirements increase above 200°C (in the 200-250°C range), Cu wires with high performance, high temperature polymer insulation (polyimide or Teflon) would still be acceptable but the MPP and Sendust cores are no longer within range. If this occurs, higher temperature core materials will be considered.

Resistors

Resistance value, temperature coefficient of resistance (TCR) or change in resistance with temperature, noise, and maximum recommended current or power are all important in the selection of resistors. Due to the reduced thermal conductivity combined with the high temperatures of the environment, the maximum current or power must be derated. In addition, the placement of resistors with respect to other components needs to be taken into account for the circuit design, since these high power dissipating resistors may be survivable at higher temperatures than the components that surround them. Nevertheless, various resistors are available that can be used to 300°C, with some being used as high as 500°C. Although low TCRs are often favorable for the temperature of interest, this is generally not a problem when the behavior is well known and compensated for in the design of the circuit. Changes in resistance with time at temperature; however, can change the circuit functionality over time. Finally, thermal stress between different layers of the device as well as interdiffusion and oxidation of materials are sources of concern. For each type of resistor discussed, selection of resistive material, encapsulation material and processing conditions are all important, as are the thermal exposure history and conditions [9].

Of the different types of resistors, metallized/carbon film, wirewound, thin film and thick film resistors will be discussed with respect to the impact of high temperature exposure. Metallized and carbon film resistors are limited to operation below 165°C due to sublimation of the resistive elements and softening of the epoxy coatings (which can result in separation between the encapsulant and the endcap). The more robust, large sized wirewound resistors, made from heat resistant wire and ceramic, can be used well above 200°C and are simply limited by the degradation (loss of insulation resistance and fatigue fracture) of their vitreous enamel coatings, which perform well to 300°C. Discrete and embedded thick and thin film resistors provided the most miniaturized solutions for high temperature operation. Produced by deposition, patterning and oxidation (to form a protective coating layer) of thin metal films on silicon or ceramic substrates, thin film

resistors provide high resolution, stability, high frequency performance, small size and low TCRs. Such resistors are most often made from tantalum, tantalum nitride, nickel chromium, titanium and cermets. Long term high temperature survivability is dependent upon the material used, but each of those mentioned is capable of operation above 200°C. The presence of oxygen may influence the aging of these materials. Thick film resistors are produced using proprietary ink formulations made from palladium, ruthenium, iridium and rhenium, with ruthenium silver, palladium silver and ruthenium oxide being the most often used resistive materials. Ruthenium oxide is resistant to degradation in air to 1000°C, and exhibits low TCR, good stability and low noise. Stresses generated at the interface between the substrate and the resistor due to CTE mismatches and thermal or power cycling remains a concern [8-9].

For the present project, embedded resistors will be used on the ceramic substrates. Surface mount resistors designed for high temperature operation will be used for the printed circuit boards and where needed on the ceramic substrates.

Space Qualification

One of the key elements of the HTB PPU is the high temperature operation, which is estimated at a temperature higher than 150°C at device junction from the initial study. The temperature range defined by military specifications, however, is -55°C to 125°C and, therefore, none of the existing military standards or any other industrial standards addresses the electronics and packaging reliability qualifications under the operating temperature range of the proposed HTB PPU. In addition, the effects of the combination of the high temperature and radiation environments need to be investigated as well.

Military standards apply a stress-test-driven reliability qualification approach. Historically developed to meet the requirements of military or space applications and communications equipment, this approach is intended for long life times. In addition, any field failure could be mission or life critical and thus are either not able to be repaired or are expensive to replace. The stress-test-driven reliability qualification is a go or no-go approach, which is based on a standardized set of stress tests as acceptance tests. Another reliability qualification approach is a knowledge-based approach. It differs from the stress-test-driven approach in that it comprehends additional sources of information into the qualification process, which requires the knowledge of the applications, use conditions, potential failure mechanisms, and the acceleration models for the considered failure mechanisms.

With the challenges from the new device technologies, packaging technologies, high temperature operation from the HTB PPU, a proactive approach needs to be adopted in space qualifying the HTB PPU. Combining with the stress-test-driven approach from the military standards, a design-for-reliability concept needs to be implemented to address the reliability qualification for both long term reliability and radiation effects. This requires that reliability be designed into products and processes by developing design rules using the best available science-based methods, including physics of failures, highly accelerated testing, and system reliability analysis, during the early design phase.

There are many aspects to be defined and addressed in this design-for-reliability concept with tailored military standards. One example is the derating requirements on all parts selected and used in the HBT PPU. Table 12 summarizes the derating requirements on capacitors, diodes, inductors, MOSFETs and EMI filters from MIL-STD-975M. While no existing derating standard covers the new technologies and high temperature operation, a two-step approach is proposed. The first step is to apply 0.5-0.7 electrical derating factor and 40°C margin to the qualification max rated/tested electrical bias and temperature, with the derating factor and temperature margin to be further defined and validated during the design cycles. The second step is to confirm the long term parts reliability. This will be done by reliability plotting under operating conditions with margin. In addition, we will perform PPU reliability based on application conditions and mission reliability requirements, with the required confidence level. While the first step is a tailored approach from the existing military standard, the second step requires the understanding of the technologies and the knowledge of the applications of the HTB PPU.

Table 12. Derating Requirements MIL-STD-975M

Device	Derating Requirements
Ceramic capacitors	0.6xV at <110C, 0 at >110C
Diodes	0.5xI & 0.7xV at 125C or (max-40C)
Inductors	0.5xV at (max-25C)
FETs	0.75x(V, I) & 0.5xP @ 125C (or max-40C)
EMI filters	0.5x(V, I) at 85C

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Acronyms

COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
HTB	High Temperature Boost
PMAD	Power Management and Distribution
PPU	Power Processing Unit
PWBA	Printed Wire Board Assembly
SEP	Solar Electric Propulsion
SiC	Silicon Carbon
SOA	State Of The Art

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This technical memorandum is to summarize the Formulation Study conducted during fiscal year 2012 on the High Temperature Boost (HTB) Power Processing Unit (PPU). The effort is authorized and supported by the Game Changing Technology Division, NASA Office of the Chief Technologist. NASA center participation during the formulation includes LaRC, KSC and JPL. The Formulation Study continues into fiscal year 2013. The formulation study has focused on the power processing unit. The team has proposed a modular, power scalable, and new technology enabled High Temperature Boost (HTB) PPU, which has 5-10X improvement in PPU specific power/mass and over 30% in-space solar electric system mass saving.

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