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(54) **CROSS-DIFFERENTIAL AMPLIFIER**

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This patent is subject to a terminal disclaimer.

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(22) Filed: **Jul. 29, 2011**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Division of application No. 12/686,161, filed on Jan. 12, 2010, now Pat. No. 7,999,621, which is a continuation of application No. 12/075,194, filed on Mar. 10, 2008, now Pat. No. 7,646,249, which is a continuation of application No. 11/638,639, filed on

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(51) **Int. Cl.**
H03F 3/04 (2006.01)

(52) **U.S. Cl.** **330/297**; 330/146

(58) **Field of Classification Search** 330/51, 330/146, 285, 296, 297, 298

See application file for complete search history.

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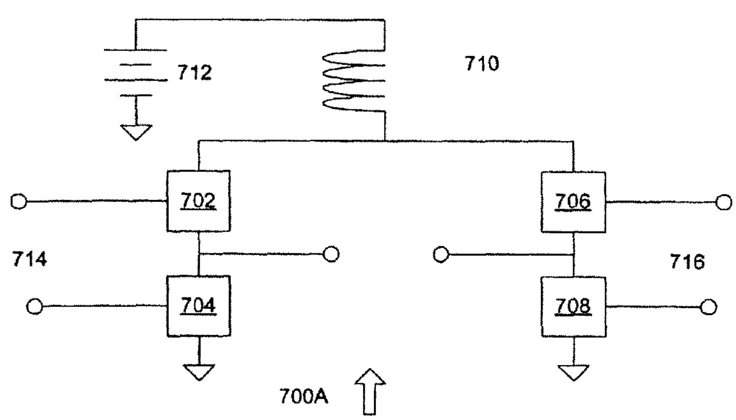
(74) *Attorney, Agent, or Firm* — Jackson Walker L.L.P.; Christopher J. Rourk

(57) **ABSTRACT**

A cross-differential amplifier is provided. The cross-differential amplifier includes an inductor connected to a direct current power source at a first terminal. A first and second switch, such as transistors, are connected to the inductor at a second terminal. A first and second amplifier are connected at their supply terminals to the first and second switch. The first and second switches are operated to commutate the inductor between the amplifiers so as to provide an amplified signal while limiting the ripple voltage on the inductor and thus limiting the maximum voltage imposed across the amplifiers and switches.

20 Claims, 7 Drawing Sheets



Related U.S. Application Data

Dec. 12, 2006, now Pat. No. 7,342,457, which is a continuation of application No. 11/208,833, filed on Aug. 22, 2005, now Pat. No. 7,157,975, which is a continuation of application No. 10/385,777, filed on Mar. 11, 2003, now abandoned.

(60) Provisional application No. 60/363,423, filed on Mar. 11, 2002.

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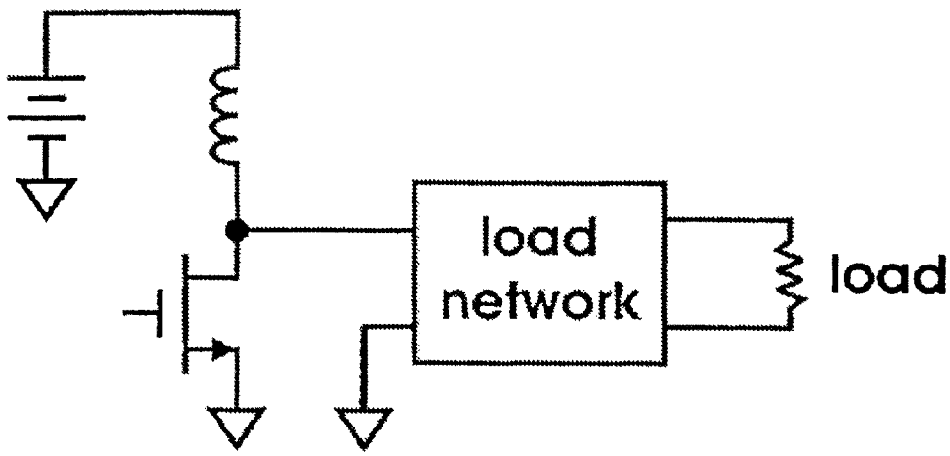


FIGURE 1

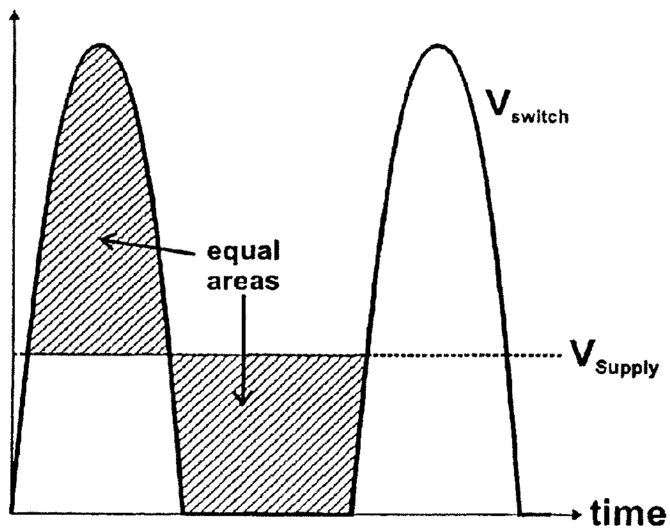


FIGURE 2

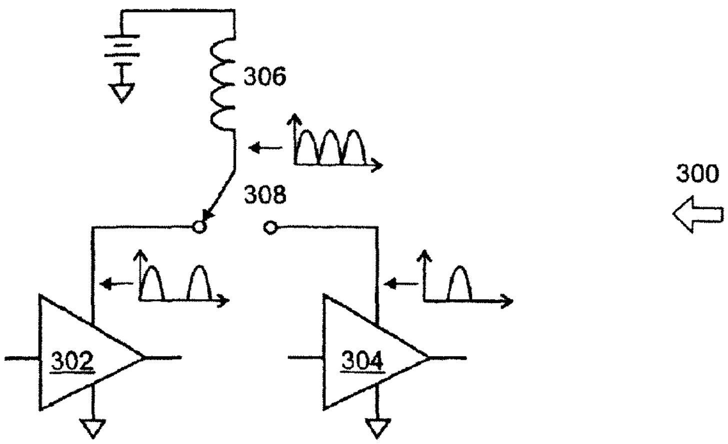


FIGURE 3

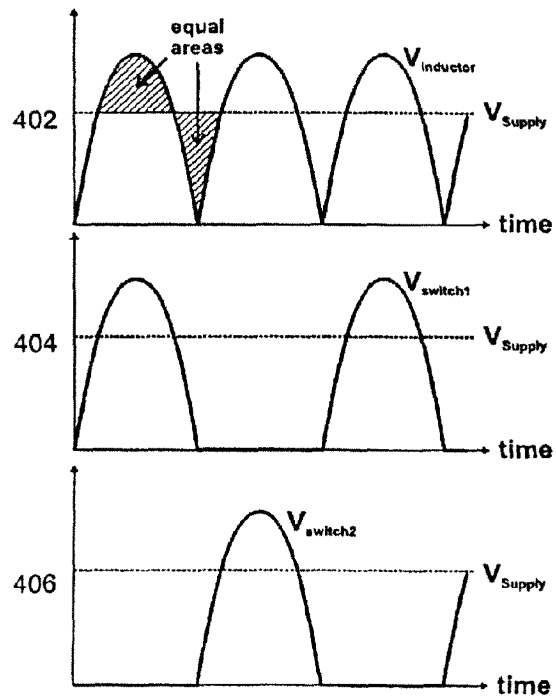


FIGURE 4

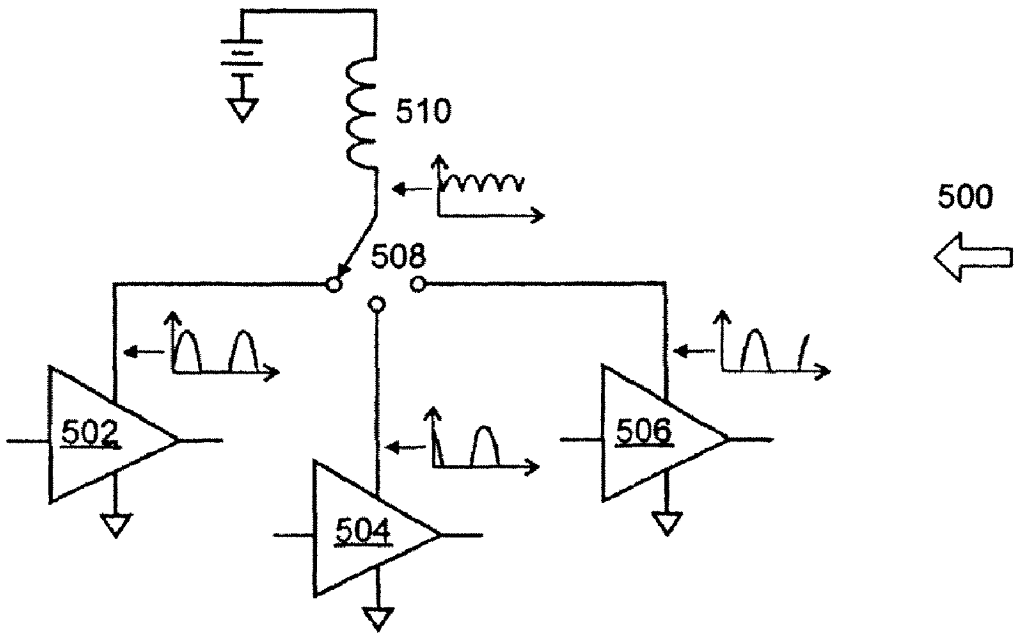


FIGURE 5

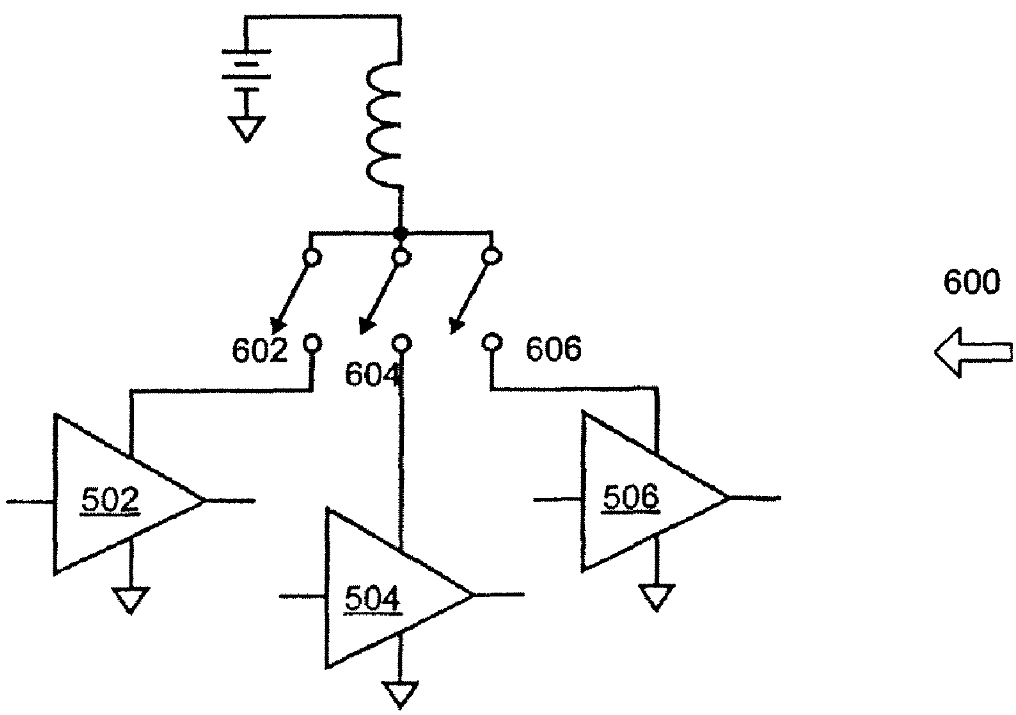
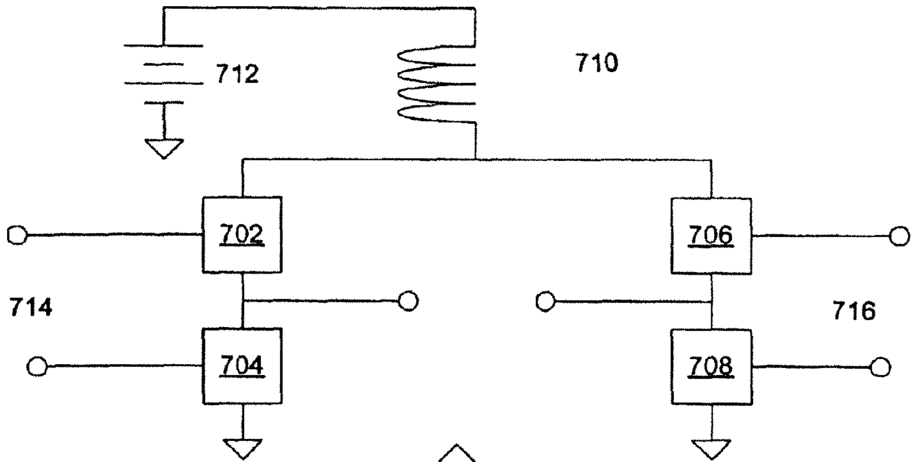
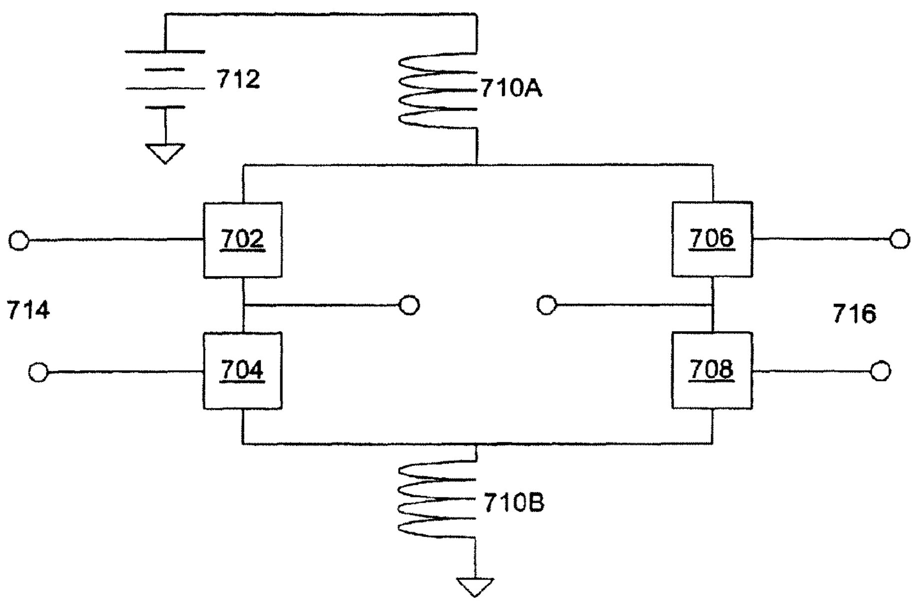


FIGURE 6



700A FIGURE 7A



700B FIGURE 7B

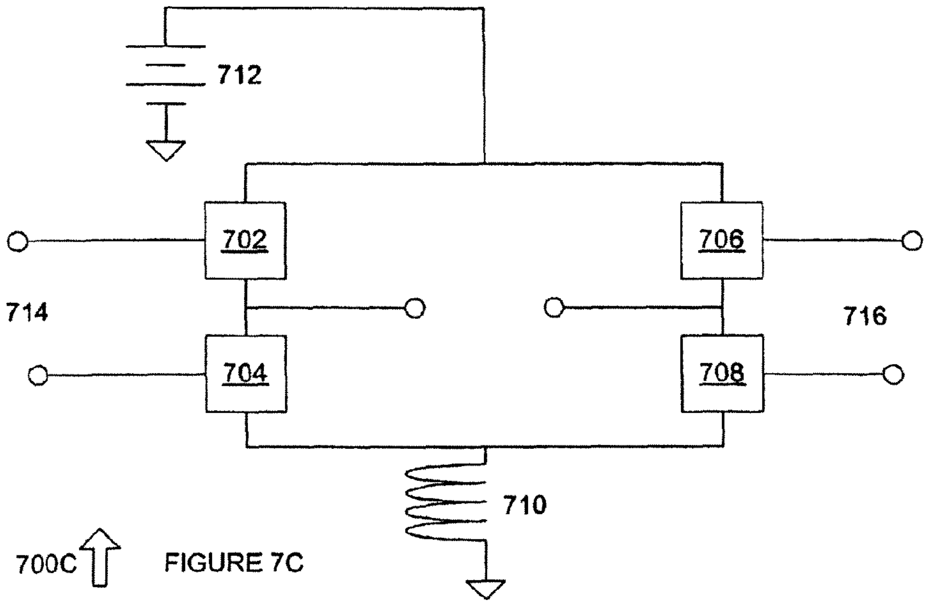


FIGURE 7C

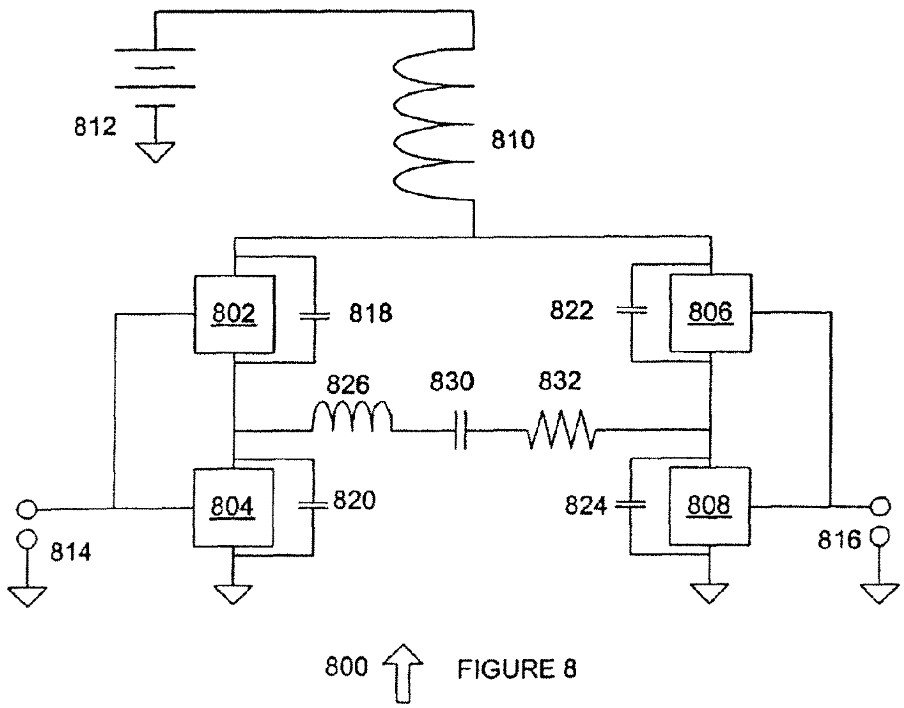


FIGURE 8

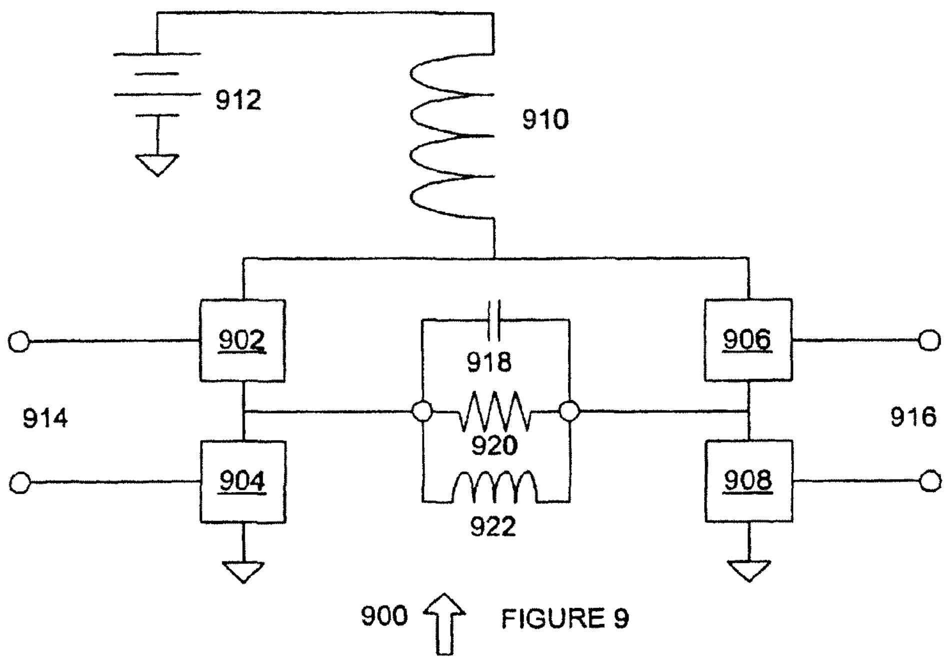


FIGURE 9

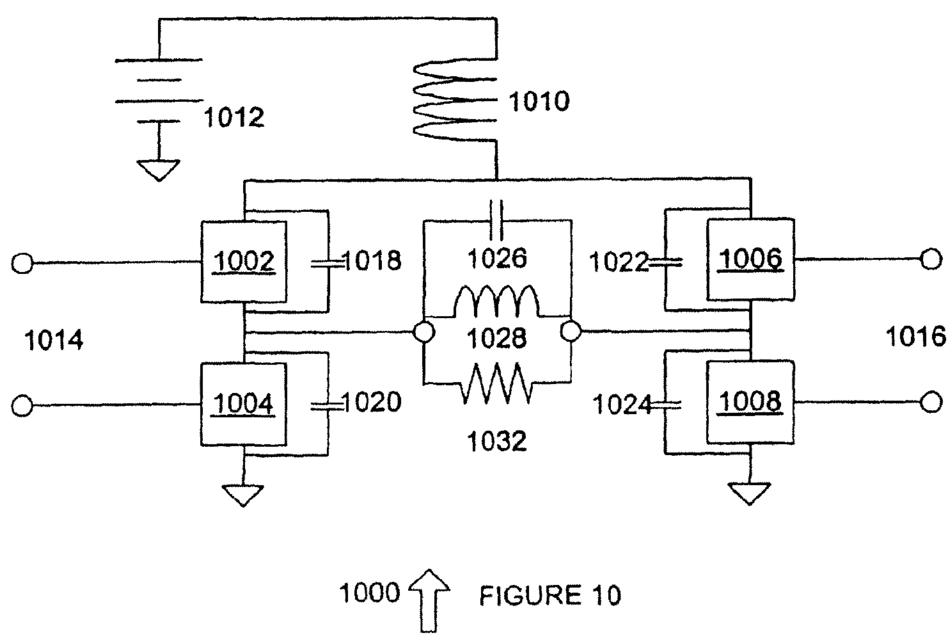


FIGURE 10

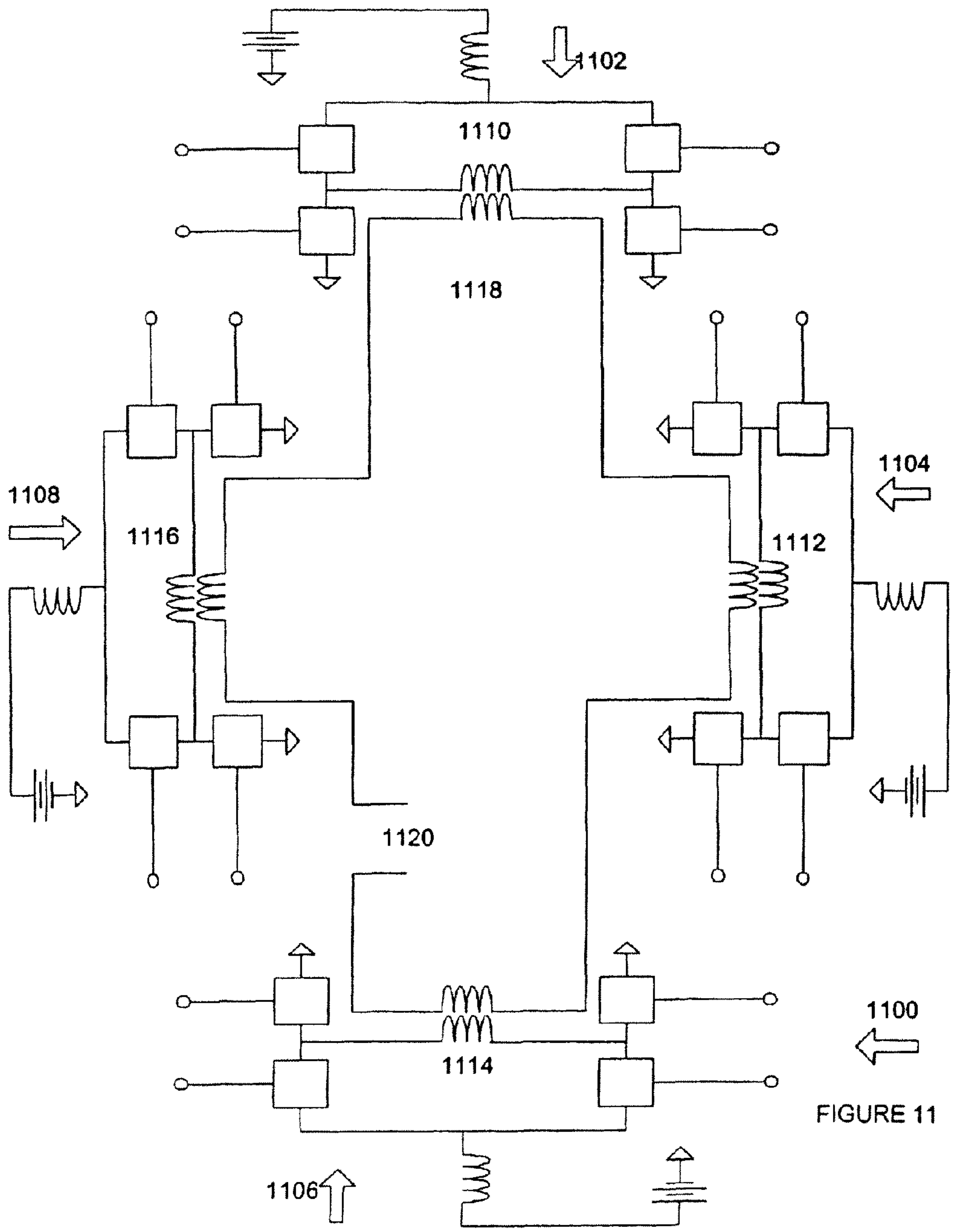


FIGURE 11

CROSS-DIFFERENTIAL AMPLIFIER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. application Ser. No. 12/686,161, "CROSS-'DIFFERENTIAL AMPLIFIER," filed Jan. 12, 2010, which is a continuation application of U.S. application Ser. No. 12/075,194, "CROSS-DIFFERENTIAL AMPLIFIER," filed Mar. 10, 2008, which is a continuation application of U.S. application Ser. No. 11/638,639, "CROSS-DIFFERENTIAL AMPLIFIER," filed Dec. 12, 2006, which is a continuation application of U.S. application Ser. No. 11/208,833, "CROSS-DIFFERENTIAL AMPLIFIER," filed Aug. 22, 2005, which is related to U.S. application Ser. No. 09/974,447, "CLASS E/F SWITCHING POWER AMPLIFIERS," filed Oct. 9, 2001. This application is also a continuation application of U.S. application Ser. No. 10/385,777, and claims priority to provisional U.S. application No. 60/363,423, filed Mar. 11, 2002, each of which are expressly incorporated by reference herein for all purposes.

The U.S. Government has certain rights to this invention pursuant to Grant No. DAAG55-97-1-0254 awarded by the Army and Grant No. NPO 30176 awarded by NASA.

FIELD OF THE INVENTION

The present invention pertains to the field of amplifiers. More specifically, the invention relates to a cross-differential amplifier that can operate at higher supply voltages.

BACKGROUND OF THE INVENTION

High efficiency saturated amplifiers and switching power amplifiers are known in the art. One drawback with the use of such amplifiers is the high peak voltages relative to the dc supply that the active devices must withstand in these modes of operation. In order to improve the gain, switching speed, and on-resistance of transistors, the breakdown voltage of the device is usually reduced. This tradeoff is exhibited by all modern semiconductor device technologies, including but not limited to field-effect transistors (FET), bipolar junction transistors (BJT), heterojunction bipolar transistors (HBT), high electron mobility transistors (HEMT), metal-semiconductor field-effect transistors (MESFET), metal-oxide semiconductor field effect transistors (MOSFET), and junction field-effect transistors (JFET). The effect is also independent of the semiconductor material system from which the devices are constructed, including but not limited to gallium arsenide (GaAs), indium phosphide (InP), silicon-germanium (SiGe), and silicon (Si) processes such as silicon bipolar (Si BJT), complementary metal oxide field effect transistor (CMOS) processes, and silicon-on-insulator (SOI) technologies.

In high efficiency switching amplifiers, such a reduction in breakdown voltage can be problematic. Unlike many applications in which the maximum voltage seen by any device is typically limited to the dc voltage of the power source, high efficiency switching amplifiers such as class E, class F, class inverse-F, current-mode class D and class E/F can require that the peak voltage seen by the devices be several times the dc supply. Class F, for instance, can require a peak voltage at least twice the supply voltage, whereas class E can require the device to withstand over 3.5 times the supply voltage without breaking down.

This high peak voltage relative to the dc power supply voltage applied results from the use of an inductor to connect the active device to the dc supply voltage. FIG. **1** is a diagram of a generalized circuit topology typically used in saturated and switching amplifiers such as class E, class F, and class E/F. The active device is connected to the dc supply through the inductor. Since the dc (or average) voltage drop across any inductor at steady state can be zero, the voltage waveform can have an average voltage equal to the supply voltage. This corresponds to a limitation on the waveform that the average area above the supply voltage and the area below it must be the same. This can be seen in FIG. **2**, depicting typical waveforms for a representative switching amplifier, with equal areas above and below the supply voltage shaded.

As can be seen in FIG. **2**, the active device spends a significant portion of its time in a low voltage state. This is so that the active device can conduct the bulk of its current during this time, thereby reducing the power dissipation in the device, resulting in high efficiency. Unfortunately, this results in a very large area below the supply voltage, necessitating an equally large area above it. Thus the voltage during the times when the switch is not low can be significantly greater than the supply voltage, usually by a factor of two to four.

In a typical CMOS process, for instance, the device breakdown can be less than 6 V whereas the supply voltage is in many cases 3.3 V or higher. With a 3.3 V supply, the class E amplifier can produce waveforms with peak voltage greater than 11V, almost twice that which a CMOS device with 6 V breakdown can tolerate. Thus in this application, the supply voltage can be changed, a more expensive high-voltage process can be used, or a less efficient type of power amplifier with a lower peak voltage can be employed. If the supply voltage cannot be changed, such as if it is coming from a battery or if other circuits on the same supply cannot change their supply voltage, the high peak to supply ratio of the traditional switching amplifiers thus forces a sacrifice in either cost or performance.

SUMMARY OF THE INVENTION

In accordance with the present invention, a cross-differential amplifier is provided that overcomes known problems with existing amplifiers.

In particular, a cross-differential amplifier is provided that allows devices with low breakdown voltage such as high-frequency transistors or integrated circuit transistors to be used with higher supply voltages.

In accordance with an exemplary embodiment of the present invention, a cross-differential amplifier is provided. The cross-differential amplifier includes an inductor connected to a dc power source at a first terminal. A first and second switching device, such as transistors, are connected to the inductor at a second terminal. A first and second amplifier are connected to the first and second switching devices at their supply points. The first and second switch are configured to connect the two amplifiers to the inductor in an alternating fashion so that each amplifier receives current and that the average voltage on the second terminal of the inductor is greater than the average voltage of one of the amplifiers at its supply point.

The present invention provides many important technical advantages. One important technical advantage of the present invention is an amplifier that can be used in high efficiency switching modes, such as in classes E, inverse F, E/F_{XX}, current-mode class D, and other suitable classes, while operating from higher supply voltages while using lower breakdown voltage devices.

Those skilled in the art will appreciate the advantages and superior features of the invention together with other important aspects thereof on reading the detailed description that follows in conjunction with the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. **1** is a diagram of a typical saturated or switching amplifier using an inductor for the supply connection;

FIG. **2** is a diagram of typical saturated or switching amplifier waveforms, showing the equal areas above and below the supply voltage due to the inductive supply connection;

FIG. **3** is a diagram of a cross differential amplifier in accordance with an exemplary embodiment of the present invention;

FIG. **4** is a diagram of voltage waveforms in accordance with an exemplary embodiment of the present invention;

FIG. **5** is a diagram of a cross differential amplifier with three commutated amplifiers in accordance with an exemplary embodiment of the present invention;

FIG. **6** is a diagram of a cross differential amplifier with several two terminal switches used to implement the n-way commutation switch in accordance with an exemplary embodiment of the invention;

FIGS. **7**A through **7**C are diagrams of cross differential amplifiers in accordance with exemplary embodiments of the present invention;

FIG. **8** is a diagram of a cross differential amplifier which can be operated in class E mode in accordance with an exemplary embodiment of the present invention;

FIG. **9** is a diagram of a cross differential amplifier which can be operated in class inverse F, current-mode class D, or class E/F_{xx} modes in accordance with an exemplary embodiment of the present invention;

FIG. **10** is a diagram of a cross differential amplifier with intrinsic capacitances and which can be operated in class inverse F, current-mode class D, or class E/F_{xx} modes in accordance with an exemplary embodiment of the present invention;

FIG. **11** is a diagram of a distributed active transformer in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the description that follows like parts are marked throughout the specification and drawings with the same reference numerals, respectively. The drawing figures are not necessarily to scale and certain features can be shown in somewhat generalized or schematic form in the interest of clarity and conciseness.

FIG. **3** is a diagram of a cross differential amplifier **300** in accordance with an exemplary embodiment of the present invention. Cross differential amplifier **300** can include two amplifying sections **302** and **304**, which share common supply inductor **306** through two-way switch **308**. Amplifying sections **302** and **304** are driven with different phases relative to one another so that their peak voltages occur at different times. By commutating supply inductor **306** between amplifying sections **302** and **304**, the average voltage at the terminal of supply inductor **306** is greater than the average voltage of the individual amplifying sections **302** and **304**.

For instance, in one exemplary implementation, the two amplifying sections **302** and **304** are driven in a complementary fashion, with supply inductor **306** connection switched so as to keep the amplifying section **302** or **304** which has a high voltage connected to supply inductor **306**. In one exemplary embodiment, this operation produces the waveforms **402** through **406** of FIG. **4**. Since supply inductor **306** is not exposed to the low voltage of the amplifying section **302** and **304** cycles in this exemplary embodiment, the area below the dc supply voltage on the inductor voltage waveform **402** is significantly reduced. This allows the area above the dc supply to be reduced, reducing significantly the peak voltage. If the amplifying sections **302** and **304** are switching amplifiers so that the voltage in the conducting cycle of each amplifying section is nearly zero, the cross differential technique can result in a factor of two decrease in the peak voltage.

FIG. **5** is a diagram of three-way cross-differential amplifier **500** in accordance with an exemplary embodiment of the present invention. By using more than two amplifiers, each with different phase, the inductor can be commutated between the three amplifying sections **502** through **506** to even further reduce the peak voltages on the amplifying sections **502** through **506**. For instance, in one exemplary embodiment three amplifying sections **502** through **506** can be used, with **120** degrees of phase separation between any two amplifying sections. This operation results in the peak voltages for the several amplifying sections **502** through **506** occurring at three different points in the cycle so that switch **508** can commutate inductor **510** to a voltage relatively close to the peak device voltage throughout the cycle.

This technique can be extended to utilize a suitable number "n" of desired amplifiers, by using an n-way switch connecting inductor **510** to "n" amplifiers with various operating phases. By using larger numbers of amplifiers, the peak voltage can be made to approach the dc power supply voltage.

FIG. **6** is a diagram of an exemplary embodiment of cross differential amplifier **600** wherein switch **508** has been implemented as "n" two terminal switches **602** through **606**. This topology allows switch **508** to be implemented by conventional two terminal switches **602** through **606**, such as transistors.

FIG. **7**A is a diagram of a cross differential amplifier **700**A in accordance with an exemplary embodiment of the present invention. In this exemplary embodiment, devices **702** and **706** are used as switches to commutate inductor **710** between devices **704** and **708**, which operate as amplifiers. The nodes where devices **702** and **706** connect to devices **704** and **708** can be used as outputs, and can drive a differential load, independent single-ended loads, or other suitable loads. Devices **702** and **706** can be operated in a complementary fashion so as to connect inductor **710** to devices **704** and **708** in an alternating fashion, so as to reduce the peak voltage on devices **704** and **708** by reducing the time that the voltage on the commutating terminal of inductor **710** is significantly lower than the supply voltage.

Device **702**, device **704**, device **706** and device **708** can be Si transistors, SiGe transistors, GaAs transistors, CMOS transistors, CMOS SOI transistors, HBT transistors, LDMOS transistors, HEMT transistors, MESFET transistors or other suitable switches or three terminal devices having a control terminal (including but not limited to a gate or base), and two conducting terminals (including but not limited to an emitter and collector or a drain and source). In one exemplary embodiment, device **704** and device **708** can be current sources having controllable current magnitude, can be switches or devices operated as switches, or can be other suitable devices. Device **702** and device **706** can be switches, devices operated as switches, or other suitable devices.

Cross differential amplifier **700**A can also be operated an that device **704** and device **708** are used as the commutating switches while using device **702** and device **706** as the amplifying devices. In this mode, device **704** and device **708** alternately force device **702** and device **706** to support the voltage at the second terminal of inductor **710**, allowing a reduction of peak voltage on device **702** and device **706** for the same dc supply voltage.

Cross differential amplifier **700**A can also be used so that all four devices are switching, so that each pair of switching amplification devices acts as a commutator for the other, or in other suitable manners.

FIG. **7**C is a diagram of a cross differential amplifier **700**C where inductor **710** has been placed at the ground side of the circuit and the supply voltage is connected directly to device **702** and device **706**. Cross differential amplifier **700**C can behave substantially like cross differential amplifier **700**A in regards to its behavior. In cross differential amplifier **700**C, device **704** and device **708** can be used as switches to connect device **702** and device **706** between supply **712** and inductor **710**, resulting in the same peak voltage reduction effect on device **702** and device **706**. In this case, the inductor is connected to ground, so that the effect is achieved by connecting devices **702** and **706** to the inductor **710** in such a way as to reduce the time that the inductor sees voltages significantly higher than ground. For instance, in one exemplary embodiment, devices **704** and **708** can be operated to commutate inductor **710** between devices **702** and **706** so as to keep the inductor connected throughout the cycle to the amplifying device which has the most negative voltage at its output terminal

Cross-differential amplifier **700**C can also be operated so that device **702** and device **706** are used as commutating switches, while using devices **704** and **708** as amplifying devices. In this mode, devices **702** and **706** alternately force the amplifying devices to support the voltage difference between the power supply voltage and the commutating point of inductor **710**, allowing a reduction of the peak voltage on devices **704** and **708**.

Cross-differential amplifier **700**C can also be used so that all four devices are switching so that each pair of amplifying switches commutates the current for the other, or in other suitable manners.

FIG. **7**B is a diagram of cross differential amplifier **700**B in accordance with an exemplary embodiment of the present invention. Cross differential amplifier **700**B includes inductor **710**A connected to device **702** and device **706**, and inductor **710**B connected to device **704** and device **708**. Since these inductors are connected in series with each other and with the dc power supply **712**, this implementation also operates substantially the same as cross differential amplifier **700**A. By using devices **702** and **706** as switches to commutate inductors **710**A and **710**B between devices **704** and **708**, which are used as amplifying devices, the voltage ripple on inductors **710**A and **710**B can be reduced, which also reduces the peak voltage seen on device **702** and **706** and devices **704** and **708** for a given dc supply voltage.

Cross-differential amplifier **700**B can also be operated so that device **704** and device **708** are used as commutating switches, while using devices **702** and **706** as amplifying devices. In this mode, devices **704** and **708** alternately force the amplifying devices to support the voltage difference between the supply inductors **710**A and **710**B, allowing a reduction of the peak voltage on devices **702** and **706**.

Cross-differential amplifier **700**B can also be used on that all four devices are switching so that each pair of amplifying switches commutates the current for the other, or in other suitable manners.

In operation, the load network and bias points for the amplifiers of cross differential amplifiers **700**A, **700**B and **700**C can be selected so as to allow operation in class A, class A/B, class B, class C, class E, inverse F, and class E/F_{xx} (signifying any class of switching amplifier operation belonging to the family of switching amplifiers E/F). An example of class E/F amplifiers is provided by U.S. application Ser. No. 09/974,557, "Class E/F Switching Power Amplifiers," filed Oct. 9, 2001, and which is hereby incorporated by reference for all purposes. Cross differential amplifiers **700**A through **700**C can be used where switching amplifier tunings are used since all four devices can be made to simultaneously operate in the high efficiency class E, inverse F, current-mode class D, and class E/F_{xx} modes.

FIG. **8** is a diagram of a cross differential amplifier **800** which can be operated in class-E mode in accordance with an exemplary embodiment of the present invention. Cross differential amplifier **800** includes device **802**, device **804**, device **806**, and device **808**, which can be operated as switches, or other suitable devices. Device **802** and device **808** can be operated as a first set in opposition to the phase of device **806** and device **804**, such that current is driven through inductor **836**, capacitor **830**, and resistor **832** in a first direction through device **802** and device **808**, and then in a second direction through device **806** and device **804**. Inductor **826**, capacitor **830**, and resistor **832** can be sized to resonate at the operating frequency, and to supply a suitable impedance at the operating frequency so as to compensate for capacitor **818**, capacitor **820**, capacitor **822**, and capacitor **824**, which can be the internal capacitances of devices **802** through **808**, respectively, or other suitable capacitances, so as to allow cross differential amplifier **800** to operate in the class-E mode of operation. In one exemplary embodiment, capacitors **818** through **824** can be the intrinsic capacitance of devices **802** through **808**, respectively, can be capacitances between devices **802** through **808** and external components or features, can be a suitable combination of such capacitances, or can include other suitable capacitors or capacitance. In another exemplary embodiment, resistor **832** can be a resistive load to be driven, the resistive component of a reactive load to be driven, an antenna, the input of an amplifier or other circuit, or other suitable loads or combinations of loads.

Using this technique, inductor **810** which is used for class E operation does not have a large voltage across it for long periods of time since it does not connect directly to ground as is the case in conventional class E amplifiers. In this manner, the peak voltage at the node shared by device **802**, device **806**, and inductor **810** is less than the peak voltage of the equivalent node of a conventional class-E switching differential amplifier such as one that uses independent inductors to connect each of the amplifying devices to the supply, or of the equivalent node of a conventional class-E switching amplifier. By selecting appropriate values for inductor **826**, capacitor **830**, resistor **832**, and capacitors **818** through **824**, each device **802** through **808** can be switched at a time when the voltage is at or close to zero, so as to minimize the turn-on switching losses due to capacitances **818** through **824** (equal to $\frac{1}{2}CV^2f_0$), and which results in undesirable power losses and heating. Cross differential amplifier **800** can also be used in the configurations shown in FIGS. **7**B and **7**C, with supply inductors in other suitable locations. Additionally, the load network can consist of the series RLC network depicted in FIG. **8**, or other suitable single-ended or differential loads meeting the class-E tunings conditions for each amplifying device.

FIG. **9** is a diagram of a cross differential amplifier **900** which can be operated in current-mode class D, class inverse F or class E/F modes of operation in accordance with an exemplary embodiment of the present invention. Cross differential amplifier **900** includes device **902**, device **904**, device **906** and device **908**, each of which can be operated as switches or other suitable devices, and inductor **910** and supply voltage **912**. Device **902** and device **908** operate in phase with each other and opposite to the phase of device **906** and device **904**, such that in the first state of operation, current flows through inductor **910** and device **902** across a load formed by capacitor **918**, resistor **920**, and inductor **922**, and through device **908**. Likewise, in the second state of operation, current flows through inductor **910** and device **906** through the load formed by capacitor **918**, resistor **920**, and inductor **922** connected in parallel, and through device **904**. Inductor **922**, capacitor **918**, and resistor **920** are selected to provide suitable tuning for current-mode class D, class inverse F or class E/F_{xx} modes of operation. In one exemplary embodiment, resistor **920** can be a resistive load to be driven, the resistive component of a reactive load to be driven, an antenna, the input of an amplifier or other circuit, or other suitable loads or combinations of loads.

Using this technique, the supply inductor **910** which can be used for current-mode class D, inverse-F and E/F_{xx} operation can avoid having large voltage across it for periods of time since it is not connected directly to ground for large portions of the cycle as is the case in conventional current-mode class D, inverse-F and E/F_{xx} amplifiers. This configuration allows the peak voltage of the node shared by the inductor **910** and devices **902** and **906** to be less than the peak voltage of the equivalent node of a conventional class inverse F or class E/F_{xx} switching differential amplifier using two inductors to connect the two devices to the voltage source, each one individually, or the equivalent node of a conventional class inverse F, current-mode class D, or class E/F_{xx} switching amplifier. Cross differential amplifier **900** can also be used in the configurations shown in FIGS. **7**B and **7**C, with supply inductors in other suitable locations. Additionally, the load network used can be a suitable single-ended or differential network which results in current-mode class D, inverse-F or E/F_{xx} operation.

FIG. **10** is a diagram of cross differential amplifier **1000** with intrinsic capacitances which can be operated in class E/F_{xx} mode in accordance with an exemplary embodiment of the present invention.

Cross differential amplifier **1000** includes device **1002**, device **1004**, device **1006**, and device **1008**, which can be operated as switches, current sources, or other suitable devices. Devices **1002** and **1006** are connected to inductor **1010**. Device **1002** and device **1008** operate in phase with each other and opposite to the phase of device **1006** and device **1004**, such that current flows in the first state of operation through inductor **1010** and device **1002** across the load formed by inductor **1028**, capacitor **1026**, and resistance **1032** through device **1008**. In the second state of operation, current flows through inductor **1010** and device **1006** and then across the load formed by capacitor **1026**, inductor **1028**, and resistance **1032** through device **1004**. Inductor **1028** and capacitor **1026** are selected to resonate at the operating frequency, and to compensate for capacitors **1018** through capacitor **1024** so as to provide class inverse F mode or class E/F_{xx} mode of operation. Capacitors **1018** through **1024** can be the intrinsic or parasitic capacitance of the devices, external capacitances, or other capacitances. Likewise, other intrinsic or parasitic capacitances of cross differential amplifier **1000** can be compensated for. In one exemplary embodiment, resistor **1032** can be a resistive load to be driven, the resistive component of a reactive load to be driven, an antenna, the input of an amplifier or other circuit, or other suitable loads or combinations of loads.

Using this technique, inductor **1010** which can be used for E/F_{xx} operation can avoid having large voltage across it for large periods of time since it is not connected directly to ground for large portions of the cycle, as is the case in conventional inverse-F and E/F_{xx} amplifiers. This configuration allows the peak voltage of the node shared by the inductor **1010** and devices **1002** and **1006** to be less than the peak voltage of the equivalent node of a conventional switching differential amplifier, such as one using two separate inductors to connect the two devices individually to the voltage source, or the equivalent node of a conventional switching amplifier. Cross differential amplifier **1000** can also be used in the configurations shown in FIGS. **7**B and **7**C, with supply inductors in other suitable locations. Additionally, the load network used can be any suitable single-ended or differential network which results in E/F_{xx} operation.

FIG. **11** is a diagram of a distributed active transformer **1100** in accordance with an exemplary embodiment of the present invention. Distributed active transformer **1100** includes cross differential amplifiers **1102**, **1104**, **1106** and **1108**, which are connected to provide primary winding segments **1110**, **1112**, **1114**, and **1116**. Secondary winding **1118** includes output **1120**, and is magnetically connected to the primary winding sections **1110** through **1116**. The current through each primary winding section is controlled by the corresponding cross differential amplifier, such that a distributed transformer architecture is provided that uses cross differential amplifiers as primary winding sections. Although four cross differential amplifiers are shown in this implementation, any suitable number of amplifying devices can be combined in the distributed active transformer. The various cross differential amplifiers can also be used in the configurations shown in FIGS. **7**B and **7**C, with inductors in other suitable locations.

Although exemplary embodiments of the system and method of the present invention has been described in detail herein, those skilled in the art will also recognize that various substitutions and modifications can be made to the systems and methods without departing from the scope and spirit of the appended claims.

What is claimed is:

1. A method for operating an amplifier circuit comprising:
- operating a first device and a second device as amplifiers to generate an output in a first mode of operation;
- operating a third device and a fourth device to commutate an inductor in the first mode of operation;
- operating the first device and the second device to commutate the inductor in a second mode of operation; and
- operating the third device and the fourth device as amplifiers to generate the output in the second mode of operation.

2. The method of claim **1** wherein the first device is operated at a radio frequency.

3. The method of claim **1** wherein the first and second devices are operated at a radio frequency.

4. The method of claim **1** wherein the first, second and third devices are operated at a radio frequency.

5. A method for operating an amplifier circuit comprising:
- operating a first device and a second device as amplifiers to generate an output in a first mode of operation;
- operating the first device and the second device as switches to commutate an inductor in a second mode of operation;
- operating a third device and a fourth device to commutate an inductor between the first device and the second device in the first mode of operation; and
- operating the third device and the fourth device as amplifiers to generate the output in the second mode of operation.

6. The method of claim 5 wherein the first device is operated at a radio frequency.

7. The method of claim 5 wherein the first and second devices are operated at a radio frequency.

8. The method of claim 5 wherein the first, second and third devices are operated at a radio frequency.

9. A method for operating an amplifier circuit comprising:
- operating a first device and a second device as amplifiers to generate an output in a first mode of operation;
- operating a third device and a fourth device as switches to commutate an inductor between the first device and the second device in the first mode of operation;
- operating the first device and the second device as switches to commutate the inductor between the third device and the fourth device in a second mode of operation; and
- operating the third device and the fourth device as amplifiers to generate the output in the second mode of operation.

10. The method of claim 9 wherein the first device is operated at a radio frequency.

11. The method of claim 9 wherein the first and second devices are operated at a radio frequency.

12. The method of claim 9 wherein the first, second and third devices are operated at a radio frequency.

13. The method of claim 1 wherein the first device and the second device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

14. The method of claim 1 wherein the third device and the fourth device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

15. The method of claim 5 wherein the first device and the second device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

16. The method of claim 5 wherein the third device and the fourth device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

17. The method of claim 9 wherein the first device and the second device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

18. The method of claim 9 wherein the third device and the fourth device are operated as one of class A amplifiers, class A/B amplifiers, class B amplifiers, class C amplifiers, class E amplifiers, inverse F amplifiers, or class E/F amplifiers.

19. The method of claim 1 wherein the first device and the second device are operated in opposition to the third device and the fourth device.

20. The method of claim 5 wherein the first device and the second device are operated in opposition to the third device and the fourth device.

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