tors (pHEMTs), in the form of monolithic microwave integrated circuits (MMICs). Since the processing of HEMT amplifiers is quite different from that of Schottky diodes, use of Schottky mixers requires separate MMICs for the mixers and amplifiers. Fabrication of all the down-/up-conversion circuitry on single MMICs, using all-HEMT circuits, would constitute a major advance in circuit simplicity.

Three pHEMT-based subharmonic 670-GHz mixers were developed that are all subharmonically pumped at about 300 GHz, which greatly simplifies the local oscillator (LO) source, compared to a fundamentally pumped mixer requiring a 600-GHz source. The mixers use an active topology. Fundamentally, they are configured as a single-stage, grounded-source amplifier with a drain load controlled by the LO. The drain load is an additional transistor, or pair of transistors, switched by the LO signal. This effectively samples the signal from the amplifier at the LO frequency, and passes the beat note on to the output terminal of the mixer.

In the down-converting mixer, the 670-GHz RF input is connected to the gate of the grounded source stage, whose drain is directly connected to the source or sources of the LO FETs (field-effect transistors). One version has only a single transistor in the drain load, and relies on the non-linearity of the FET plus the output tuning circuitry to block the RF and LO signals and passes only the IF to the output terminal.

The second down-converting mixer replaces the single LO FET with a pair having sources and drains connected together. The LO signal is fed to the two gates through a network that gives a 180° phase shift to one FET. Hence, the two FETs are switched on for alternating half-cycles of the 300-GHz LO, and the drain FET pair acts like a sampler at twice the LO frequency. Simulations indicate about 6 dB of improvement in the conversion gain, from –6 dB for the two-FET design to around 0 dB for the three-FET design.

For the up-converting mixer, the circuit is similar to the three-FET down-converter, but with the IF input going to the gate of the grounded source stage, and the RF output taken from the drains of the LO transistors. The RF and IF matching networks are also modified to the correct frequency ranges. Simulations indicate a conversion gain of about 3 dB.

This work was done by Erich T. Schlecht, Goutam Chattopadhyay, Robert H. Lin, and Seth Sin of Caltech; and William Deal, Bryan Rodriguez, Brian Bayuk, Kevin Leong, and Gerry Mei of Northrup Grumman for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-48204

Lidar Electro-Optic Beam Switch with a Liquid Crystal Variable Retarder

Lyndon B. Johnson Space Center, Houston, Texas

A document discusses a liquid crystal variable retarder, an electro-optic element that changes the polarization of an optical beam in response to a low-voltage electronic signal. This device can be fabricated so that the element creates, among other states, a half-wave of retardance that can be reduced to a very small retardance. When aligned to a polarized source, this can act to rotate the polarization by 90° in one state, but generate no rotation in the other state. If the beam is then incident on a polarization beam splitter, it will efficiently switch from one path to the other when the voltage is applied. The laser beam switching system has no moving parts, improving reliability over mechanical switching. It is low cost, tolerant of high laser power density, and needs only simple drive electronics, minimizing the required system resources.

This work was done by James Baer of Ball Aerospace & Technologies Corp. for Johnson Space Center. Further information is contained in a TSP (see page 1). MSC-25113-1

Feedback Augmented Sub-Ranging (FASR) Quantizer

This device increases the accuracy of a switched capacitor amplifier, reduces the power and area of an integrated circuit, and reduces manufacturing cost.

Goddard Space Flight Center, Greenbelt, Maryland

This innovation is intended to reduce the size, power, and complexity of pipeline analog-to-digital converters (ADCs) that require high resolution and speed along with low power. Digitizers are important components in any application where analog signals (such as light, sound, temperature, etc.) need to be digitally processed. The innovation implements amplification of a sampled residual voltage in a switched capacitor amplifier stage that does not depend on charge redistribution. The result is less sensitive to capacitor mismatches that cause gain errors, which are the main limitation of such amplifiers in pipeline ADCs. The residual errors due to mismatch are reduced by at least a factor of 16, which is equivalent to at least 4 bits of improvement. The settling time is also faster because of a higher feedback factor.

In traditional switched capacitor residue amplifiers, closed-loop amplification of a sampled and held residue signal is achieved by redistributing sampled charge onto a feedback capacitor around a high-gain transconductance amplifier. The residual charge that was sampled during the acquisition or sampling phase is stored on two or more capacitors, often equal in value or integral multiples of each other. During the hold or amplification phase, all of the charge is redistributed onto one capacitor in the feedback loop of the ampli-

fier to produce an amplified voltage. The key error source is the non-ideal ratios of feedback and input capacitors caused by manufacturing tolerances, called "mismatches." The mismatches cause non-ideal closed-loop gain, leading to higher differential non-linearity. Traditional solutions to the mismatch errors are to use larger capacitor values (than dictated by thermal noise requirements) and/or complex calibration schemes, both of which increase the die size and power dissipation.

The key features of this innovation are (1) the elimination of the need for charge redistribution to achieve an accurate closed-loop gain of two, (2) a higher feedback factor in the amplifier stage giving a higher closed-loop bandwidth compared to the prior art, and (3) reduced requirement for calibration. The accuracy of the new amplifier is mainly limited by the sampling networks' parasitic capacitances, which should be minimized in relation to the sampling capacitors.

This work was done by Gerard Quilligan of Goddard Space Flight Center. Further information is contained in a TSP (see page 1).GSC-16187-1

Real-Time Distributed Embedded Oscillator Operating Frequency Monitoring

Lyndon B. Johnson Space Center, Houston, Texas

A document discusses the utilization of embedded clocks inside of operating network data links as an auxiliary clock source to satisfy local oscillator monitoring requirements. Modem network interfaces, typically serial network links, often contain embedded clocking information of very tight precision to recover data from the link. This embedded clocking data can be utilized by the receiving device to monitor the local oscillator for tolerance to required specifications, often important in high-integrity fault-tolerant applications.

A device can utilize a received embedded clock to determine if the local or the remote device is out of tolerance by using a single link. The local device can determine if it is failing, assuming a single fault model, with two or more active links. Network fabric components, containing many operational links, can potentially determine faulty remote or local devices in the presence of multiple faults.

Two methods of implementation are described. In one method, a recovered clock can be directly used to monitor the local clock as a direct replacement of an external local oscillator. This scheme is consistent with a general clock monitoring function whereby clock sources are clocking two counters and compared over a fixed interval of time. In another method, overflow/underflow conditions can be used to detect clock relationships for monitoring. These network interfaces often provide clock compensation circuitry to allow data to be transferred from the received (network) clock domain to the internal clock domain. This circuit could be modified to detect overflow/underflow conditions of the buffering required and report a fast or slow receive clock, respectively.

This work was done by Julie Pollock, Brett Oliver, and Christopher Brickner of Honeywell, Inc. for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809.

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)}, to Honeywell, Inc. Inquiries concerning licenses for its commercial development should be addressed to:

Aerospace – Defense & Space
Honeywell
P.O. Box 52199
Phoenix, AZ 85072-2199
Phone No.: (602) 822-3000

Refer to MSC-24765-1, volume and number of this NASA Tech Briefs *issue, and the page number.*