# Pattern Generator for Bench Test of Digital Boards

**Fresh data is streamed continuously for many tens of seconds with no gaps at 40 MHz.**

*NASA's Jet Propulsion Laboratory, Pasadena, California*

All efforts to develop electronic equipment reach a stage where they need a board test station for each board. The SMAP digital system consists of three board types that interact with each other using interfaces with critical timing. Each board needs to be tested individually before combining into the integrated digital electronics system. Each board needs critical timing signals from the others to be able to operate. A bench test system was developed to support test of each board. The test system produces all the outputs of the control and timing unit, and is delivered much earlier than the timing unit.

Timing signals are treated as data. A large file is generated containing the state of every timing signal at any instant. This file is streamed out to an IO card, which is wired directly to the device-under-test (DUT) input pins. This provides a flexible test environment that can be adapted to any of the boards required to test in a standalone configuration. The problem of generating the critical timing signals is then transferred from a hardware problem to a software problem where it is more easily dealt with.

The first board to be tested was the ADC Digital Processor board (ADP). The ADP needed a complex Xilinx configuration data stream to operate, plus timing signals. The IO card is wired directly to the configuration and timing inputs of the board through VME connectors. A slower pattern maker program combines the Xilinx configuration and desired timing into a large data file. This data file is clocked out at 40 MHz (32 bits of data) into 28 inputs of the ADP to make it run.

The formatter board needs data from an ADP, plus timing information from the control and timing unit. Data captured from the ADP in its standalone test is combined with timing information into a large file. The large file streams out the IO card and is wired to formatter inputs. Since the formatter has more inputs than the IO card has bits, several signals were cross-strapped (duplicated), making it appear to the formatter that it was receiving two ADP boards when it was in fact receiving two copies of the same ADP board. In combined ADP/formatter integration, the IO card emulates the timing unit only.

Using IO cards to emulate missing hardware for bench test is an older technology. The improvement here is the ability to stream out fresh data continuously for many tens of seconds with no gaps at 40 MHz. This allows precise control over timing with time tag information that varies over a wide range. This allows a much better bench test than would have been possible in short pulses.

By allowing more complete testing of the individual boards when they are ready rather than deferring test to integration, the delivery of the SMAP digital system is accelerated.

*This work was done by Andrew C. Berkun and Anhua J. Chu of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).*

*The software used in this innovation is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. Refer to NPO-48231.*

# 670-GHz Down- and Up-Converting HEMT-Based Mixers

**Applications include passive, active, or radar imaging.**

*NASA's Jet Propulsion Laboratory, Pasadena, California*

A large category of scientific investigation takes advantage of the interactions of signals in the frequency range from 300 to 1,000 GHz and higher. This includes astronomy and atmospheric science, where spectral observations in this frequency range give information about molecular abundances, pressures, and temperatures of small-sized molecules such as water. Additionally, there is a minimum in the atmospheric absorption at around 670 GHz that makes this frequency useful for terrestrial imaging, radar, and possibly communications purposes. This is because 670 GHz is a good compromise for imaging and radar applications between spatial resolution (for a given antenna size) that favors higher frequencies, and atmospheric losses that favor lower frequencies. A similar trade-off applies to communications link budgets: higher frequencies allow smaller antennas, but incur a higher loss.

All of these applications usually require converting the RF (radio frequency) signal at 670 GHz to a lower IF (intermediate frequency) for processing. Further, transmitting for communication and radar generally requires up-conversion from IF to the RF. The current state-of-the-art device for performing the frequency conversion is based on Schottky diode mixers for both up and down conversion in this frequency range for room-temperature operation. Devices that can operate at room temperature are generally required for terrestrial, military, and planetary applications that cannot tolerate the mass, bulk, and power consumption of cryogenic cooling.

The technology has recently advanced to the point that amplifiers in the region up to nearly 1,000 GHz are feasible. Almost all of these have been based on indium phosphide pseudomorphic high-electron mobility transis-

tors (pHEMTs), in the form of monolithic microwave integrated circuits (MMICs). Since the processing of HEMT amplifiers is quite different from that of Schottky diodes, use of Schottky mixers requires separate MMICs for the mixers and amplifiers. Fabrication of all the down-/up-conversion circuitry on single MMICs, using all-HEMT circuits, would constitute a major advance in circuit simplicity.

Three pHEMT-based subharmonic 670-GHz mixers were developed that are all subharmonically pumped at about 300 GHz, which greatly simplifies the local oscillator (LO) source, compared to a fundamentally pumped mixer requiring a 600-GHz source. The mixers use an active topology. Fundamentally, they are configured as a single-stage, grounded-source amplifier with a drain load controlled by the LO. The drain load is an additional transistor, or pair of transistors, switched by the LO signal. This effectively samples the signal from the amplifier at the LO frequency, and passes the beat note on to the output terminal of the mixer.

In the down-converting mixer, the 670-GHz RF input is connected to the gate of the grounded source stage, whose drain is directly connected to the source or sources of the LO FETs (field-effect transistors). One version has only a single transistor in the drain load, and relies on the non-linearity of the FET plus the output tuning circuitry to block the RF and LO signals and passes only the IF to the output terminal.

The second down-converting mixer replaces the single LO FET with a pair having sources and drains connected together. The LO signal is fed to the two gates through a network that gives a 180° phase shift to one FET. Hence, the two FETs are switched on for alternating half-cycles of the 300-GHz LO, and the drain FET pair acts like a sampler at twice the LO frequency. Simulations indicate about 6 dB of improvement in the conversion gain, from –6 dB for the two-FET design to around 0 dB for the three-FET design.

For the up-converting mixer, the circuit is similar to the three-FET down-converter, but with the IF input going to the gate of the grounded source stage, and the RF output taken from the drains of the LO transistors. The RF and IF matching networks are also modified to the correct frequency ranges. Simulations indicate a conversion gain of about 3 dB.

*This work was done by Erich T. Schlecht, Goutam Chattopadhyay, Robert H. Lin, and Seth Sin of Caltech; and William Deal, Bryan Rodriguez, Brian Bayuk, Kevin Leong, and Gerry Mei of Northrup Grumman for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).* NPO-48204

## Lidar Electro-Optic Beam Switch with a Liquid Crystal Variable Retarder

*Lyndon B. Johnson Space Center, Houston, Texas*

A document discusses a liquid crystal variable retarder, an electro-optic element that changes the polarization of an optical beam in response to a low-voltage electronic signal. This device can be fabricated so that the element creates, among other states, a half-wave of retardance that can be reduced to a very small retardance. When aligned to a polarized source, this can act to rotate the polarization by 90° in one state, but generate no rotation in the other state. If the beam is then incident on a polarization beam splitter, it will efficiently switch from one path to the other when the voltage is applied. The laser beam switching system has no moving parts, improving reliability over mechanical switching. It is low cost, tolerant of high laser power density, and needs only simple drive electronics, minimizing the required system resources.

*This work was done by James Baer of Ball Aerospace & Technologies Corp. for Johnson Space Center. Further information is contained in a TSP (see page 1).* MSC-25113-1

## Feedback Augmented Sub-Ranging (FASR) Quantizer

**This device increases the accuracy of a switched capacitor amplifier, reduces the power and area of an integrated circuit, and reduces manufacturing cost.**

*Goddard Space Flight Center, Greenbelt, Maryland*

This innovation is intended to reduce the size, power, and complexity of pipeline analog-to-digital converters (ADCs) that require high resolution and speed along with low power. Digitizers are important components in any application where analog signals (such as light, sound, temperature, etc.) need to be digitally processed. The innovation implements amplification of a sampled residual voltage in a switched capacitor amplifier stage that does not depend on charge redistribution. The result is less sensitive to capacitor mismatches that cause gain errors, which are the main limitation of such amplifiers in pipeline ADCs. The residual errors due to mismatch are reduced by at least a factor of 16, which is equivalent to at least 4 bits of improvement. The settling time is also faster because of a higher feedback factor.

In traditional switched capacitor residue amplifiers, closed-loop amplification of a sampled and held residue signal is achieved by redistributing sampled charge onto a feedback capacitor around a high-gain transconductance amplifier. The residual charge that was sampled during the acquisition or sampling phase is stored on two or more capacitors, often equal in value or integral multiples of each other. During the hold or amplification phase, all of the charge is redistributed onto one capacitor in the feedback loop of the ampli-