

semiconductor lasers could be solder-attached in modular fashion to the heat pipe, or could be made directly from the heat pipe structure itself for increased thermal efficiency. Another example would be the fabri-

cation of solar cells for use in concentrated solar collectors; co-fabrication of the heat pipe with the solar cells from the same silicon wafer would enable more efficient thermal management.

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Adaptive Phase Delay Generator

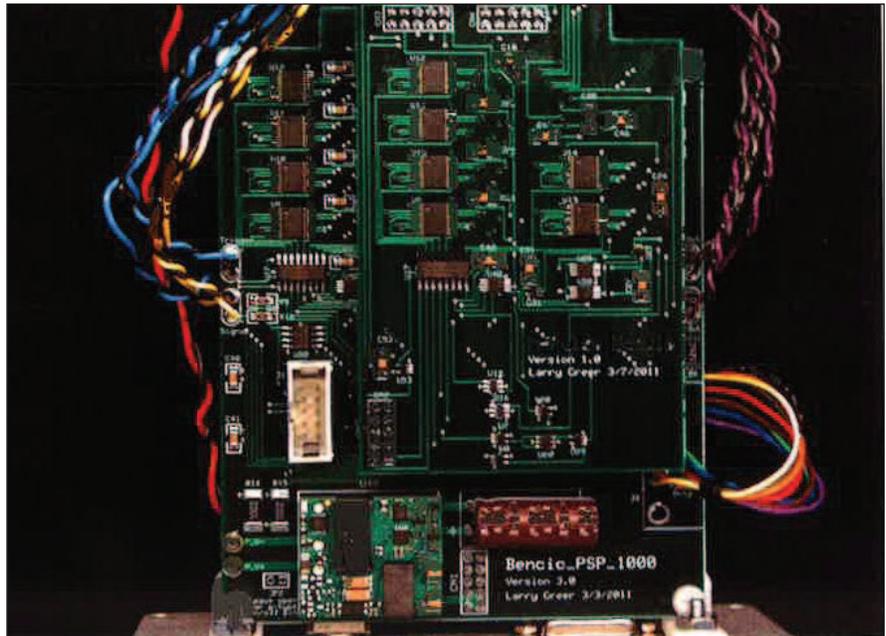
Test facilities that need to synchronize test equipment with rotating machinery could make use of this device.

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There are several experimental setups involving rotating machinery that require some form of synchronization. The adaptive phase delay generator (APDG) — the Bencic-1000 — is a flexible instrument that allows the user to generate pulses synchronized to the rising edge of a tachometer signal from any piece of rotating machinery. These synchronized pulses can vary by the delay angle, pulse width, number of pulses per period, number of skipped pulses, and total number of pulses. Due to the design of the pulse generator, any and all of these parameters can be changed independently, yielding an unparalleled level of versatility.

There are two user interfaces to the APDG. The first is a LabVIEW program that has the advantage of displaying all of the pulse parameters and input signal data within one neatly organized window on the PC monitor. Furthermore, the LabVIEW interface plots the rpm of the two input signal channels in real time. The second user interface is a handheld portable device that goes anywhere a computer is not accessible. It consists of a liquid-crystal display and keypad, which enable the user to control the unit by scrolling through a host of command menus and parameter listings.

The APDG combines all of the desired synchronization control into one unit. The experimenter can adjust the delay, pulse width, pulse count, number of skipped pulses, and produce a specified number of pulses per revolution. Each of these parameters can be changed independently, providing an unparalleled level of versatility when synchronizing



The construction of the **Adaptive Phase Delay Generator** allows for inclusion of multi-pulse functions by adding an expansion board to each channel.

hardware to a host of rotating machinery. The APDG allows experimenters to set up quickly and generate a host of synchronizing configurations using a simple user interface, which hopefully leads to faster results.

The heart of the Bencic-1000 is a reconfigurable pulse-generating state machine that cycles through three to four primary states, depending on the mode of operation. A second state machine tracks the period of the input signal by incorporating a latching synchronous 32-bit counter and a microcontroller. These hardware state machines make

use of high-speed CMOS technology, primarily from the HC family of parts, and have no problem operating with the 10-MHz master clock. The microcontroller is a 50-MHz 8051 derivative optimized to run at 50 MIPS.

This work was done by Lawrence Greer of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18942-1.