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Joint Lead-Free Solder Test Program for High Reliability Military and Space Applications

JG-PP/JCAA Lead-Free Solder Project

Abstract

Current and future space and defense systems face potential risks from the continued use of tin-lead solder, including: compliance with current environmental regulations, concerns about potential environmental legislation banning lead-containing products, reduced mission readiness, and component obsolescence with lead surface finishes. For example, the United States Environmental Protection Agency (USEPA) has lowered the Toxic Chemical Release reporting threshold for lead to 100 pounds. Overseas, the Waste Electrical and Electronic Equipment (WEEE) and the Restriction on Hazardous Substances (RoHS) Directives in Europe and similar mandates in Japan have instilled concern that a legislative body will prohibit the use of lead in aerospace/military electronics soldering. Any potential banning of lead compounds could reduce the supplier base and adversely affect the readiness of missions led by the National Aeronautics and Space Administration (NASA) and the U.S. Department of Defense (DoD). Before considering lead-free electronics for system upgrades or future designs, however, it is important for the DoD and NASA to know whether lead-free solders can meet their systems' requirements. No single lead-free solder is likely to qualify for all defense and space applications. Therefore, it is important to validate alternative solders for discrete applications.

As a result of the need for comprehensive test data on the reliability of lead-free solders, a partnership was formed between the DoD, NASA, and several original equipment manufactures (OEMs) to conduct solder-joint reliability (laboratory) testing of three lead-free solder alloys on newly manufactured and reworked circuit cards to generate performance data for high-reliability (IPC Class 3) applications.

Introduction

The use of conventional tin-lead (Sn/Pb) solder in circuit board manufacturing is under ever-increasing political scrutiny due to environmental issues and increasing regulations concerning lead. The USEPA has cited lead and lead compounds as one of the top 17 chemicals imposing the greatest threat to human health. The "Restriction of Hazardous Substances" (RoHS) directive enacted by the European Union (EU) and a pact between the United States' National Electronics Manufacturing Initiative (NEMI), Europe's Soldertec at Tin Technology Ltd. and Japan's Japan Electronics and Information Technology Industries Association (JEITA) are just two examples where worldwide legislative actions and partnerships/agreements are affecting the electronics industry. As a result, many global commercial grade electronic component manufacturers are initiating efforts to transition to lead free in order to retain their worldwide market. Lead-free components will be finding their way into the inventory of aerospace or military assembly processes under government acquisition reform initiatives. These actions will result in increased risks associated with manufacturing and subsequent repair of military electronic systems.

Starting in 2001, the USEPA lowered the Toxic Release Inventory (TRI) reporting threshold for lead to 100 pounds annually. Previously, facilities were not required to report releases of lead and lead compounds unless they manufactured or processed more than 25,000 pounds annually, or used more than 10,000 pounds a year. This requirement affects federal facilities, which, under Executive Order 12856, must file annual Toxic Release Inventory reports if they meet the threshold requirements.

The commercial sector is driving component and board suppliers to provide primarily lead-free compatible surface finishes and alloys. If the military electronics industry does not proactively participate in determining the impact of lead-free solders, it is possible that parts with lead-containing finishes may become impossible to procure or acquisition costs for "military lead containing components" will become prohibitive. Military and space applications are typically more severe than traditional commercial electronic applications. IPC defines three performance classes for surface mount assemblies, which are based on end use. IPC-6011 spells out performance classes for printed wiring boards. Class 1, *General*

Electronic Products, includes consumer products, some computer and computer peripherals suitable for applications where the major requirement is function of the completed printed board. Class 2, *Dedicated Service Electronic Products,* includes communications equipment, sophisticated business machines, instruments where high performance and extended life is required and for which uninterrupted service is desired but not critical. Class 3, *High Reliability Electronic Products,* includes the equipment and products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated and must function when required such as in life support items or flight control systems. Printed boards in this class are suitable for applications where high levels of assurance are required and service is essential [1].

While work has been done to determine lead-free reliability for Class 1 and Class 2 applications, there has been little comprehensive data published on Class 3 surface mount assemblies. To resolve the need for better understanding how lead-free solders perform under harsh environments, a joint project was initiated by the DoD's Joint Group on Pollution Prevention (JG-PP) in 2001 to characterize the performance of lead-free solders as potential replacements for conventional tin-lead solders used on printed wiring assemblies (PWAs).

The Joint Council on Aging Aircraft (JCAA), via USAF Aging Aircraft Division, assumed the role of government project manager from the JG-PP in May 2003. The JCAA is composed of primary members including Air Force Aging Aircraft, Army AMCOM, Navy Aging Aircraft, Coast Guard Aging Aircraft, DLA Aging Aircraft, FAA Aging Aircraft and adjunct members including NASA, Marine Corps, and Academia. The primary objectives of the JCAA are to field products to improve the availability and affordability of aging aeronautical systems. The reason for this project leadership change was that the JG-PP Working Group lead-free solder project encompasses much more than the pollution prevention goals established by the JG-PP. Alternatively, the JCAA saw the value of the lead-free solder project with regard to the numerous logistical and repair issues currently ongoing through out the aircraft and assets owned and maintained by the DoD and NASA. The JCAA at the director level have agreed to take over managing the lead-free solder project.

The intent of the study is to test for functional (electrical) reliability of representative test boards assembled and reworked with lead-free solders. "Representative" was defined as circuits now on defense/space systems (surface mount technology, plated through hole, and mixtures of old and new components). In addition, a portion of the test vehicles built for the lead-free solder project will test the effectiveness of repairing lead-containing printed wiring boards (PWBs) with lead-free solder.

Background

In 2001, a joint group led by the JG-PP and project technical representatives identified engineering, performance and operational impact (supportability) requirements for circuit card assemblies manufactured and reworked with lead-free solder alloys. The joint group consisted of technical representatives from the affected defense and space programs, DoD sustainment community, and other government and contractor organizations. The team reached consensus regarding the tests, procedures, methodologies and acceptance criteria to qualify alternatives against the identified requirements. The team documented these critical technical and performance requirements and tests in a Joint Test Protocol (JTP) [2].

A subsequent Joint Test Report (JTR) will document the data and results of testing. The JTP and JTR will be available to other government and commercial users for guidance on future pollution prevention efforts. Engineering authorities can refer to the test results during design decisions for specific defense and space systems. However, the tests and criteria defined in this JTP were developed by consensus only for the defense and space system programs involved, and may not address all areas of application.

Materials Selection

Solder Alloy [3]

Due to increasingly stringent regulations concerning the use of solders and component finishes containing lead, research efforts have focused on testing lead-free alternatives that would replace conventional SnPb processes for electronic applications. A set of requirements and acceptable criteria for selecting lead-free alternatives provided by project stakeholders and technical representatives was compiled.

Members of the project team identified desirable properties that lead-free solder alloys should exhibit. These requirements encompassed operational, performance, and environmental needs.

Requirements and Acceptable Criteria of Potential Alternative Solder Alloys [3]

Candidate Alloy Requirements	Acceptable Criteria
Operational Requirements	Manufacturability – Use existing equipment *Metal price – Low cost. As close to SnPb solder cost as possible.*
Engineering and Performance Requirements-	Acceptable physical properties (strength, elongation, fatigue) – Alloy must be capable of providing the mechanical strength and reliability equal to or greater than SnPb solder. Adequate electrical conductivity Adequate thermal conductivity Compatibility with lead Repeatability – Consistency in melting point Melting point – Near eutectic melting point below 260°C for wave and below 250°C (preferably around 220°C) for reflow.
ESOH Requirements	No element with an ESOH hazard equal to or greater than lead
Ingredients	No lead
Availability	Commercial availability must be able to sustain industry-wide use

ESOH = Environmental, Safety, and Occupational Health
Eutectic = the alloy composition at which a solder alloy melts/freezes completely without going through a pasty (partially solid) phase [4].

Next, the team conducted a technical survey to identify potential lead-free alternatives. The survey included literature searches, electronic database and Internet searches, technical representatives' input, and data from previous studies performed on lead-free alloys by the National Center for Manufacturing Sciences (NCMS), NEMI, and other research groups. The project consortium identified potential alloys for each of the three soldering processes (wave, reflow, and manual). The reference alloy will be eutectic 63Sn37Pb (wt-%) solder.

Selected Lead-Free Solder Alloys for Testing

Alloy	Soldering Method Used	Melting Temperature
Sn37Pb	Wave, reflow, manual	183°C (361°F)
Sn0.7Cu0.05Ni	Wave, manual	227°C (441°F)
Sn3.9Ag0.6Cu	Wave, reflow, manual	218°C (424°F)
Sn3.4Ag1Cu3.3Bi	Reflow, manual	202-214°C (396-417°F)

Sn = Tin; Pb = Lead; Ni = Nickel; Ag = Silver; Cu = Copper; Bi = Bismuth

Except where otherwise indicated, the component elements in each alloy shall not deviate from their nominal mass percentage by more than 0.20% of the alloy mass when their nominal percentage is equal to or less than 5.0%; or by more than 0.50% when their nominal percentage is greater than 5.0% [4].

Sn0.7Cu0.05Ni
This alloy is commercially available and the general trend in industry has been switching to the nickel stabilized tin-copper alloy over standard tin-copper due to superior performance. In addition, this nickel-stabilized alloy does not require special solder pots and has shown no joint failures in specimens with over 4 years of service. The cost of this alloy in the form of bar solder is relatively low when compared to other lead-free solder alloys in bar form.

This alloy was not selected for reflow applications because the higher melting temperature makes it undesirable. In addition, reflow processing requires higher temperatures than wave soldering application further increasing the temperatures required to process this alloy. Component damage due to high temperature requirements was a concern.

Sn3.9Ag0.6Cu
SnAgCu solder alloys are believed to be the leading choice of the electronics industry for lead-free solder. The Sn3.9Ag0.6Cu is recommended by NEMI and other industry and research consortia as a prime candidate for replacing SnPb solder. Sn3.9Ag0.6Cu is commercially available and currently used in electronic applications. It has been determined that alloys with compositions within the range of Sn3.5-4Ag0.5-1.0Cu all have a liquidus temperature around 217°C and have similar microstructures and mechanical properties.

This alloy was chosen for all three types of soldering (wave, reflow and manual) because this particular solder alloy has shown the most promise as a primary replacement for tin-lead solder. The team decided that they wanted to select at least one "general purpose" alloy to be evaluated against all three soldering methods and it was determined that the SnAgCu solder alloy would best serve this purpose. Conclusions drawn from literature suggest that this alloy has good mechanical properties and may be as reliable as SnPb in some applications.

Sn3.4Ag1.0Cu3.3Bi
This alloy was chosen because bismuth has been shown to enhance the long-term thermal cycle reliability of the solder joint; the Sn3.4Ag1.0Cu3.3Bi alloy was the best performer (for reflow and manual soldering) in the 2001 NCMS study. The team also wanted to include the Sn3.4Ag1.0Cu3.3Bi alloy in the test plan to see if Bi alloys adversely affect solder joint reliability when contaminated with lead. Sn3.4Ag1.0Cu3.3Bi was not selected for wave soldering in part because of the potential for fillet lifting.

Board Finish [3]

Suitable board finishes for use with SnPb and lead-free solders include immersion silver, organic solderability preservative (OSP), immersion tin and electroless nickel/immersion gold (ENIG). Each surface finish has its advantages and limitations. For example, ENIG is susceptible to "black pad" which can cause premature failure of solder joints. Immersion tin and OSP become non-solderable after several exposures to reflow conditions and OSP exhibits poor wetting with some solders.

Project stakeholders and participants selected immersion silver as the surface finish for the manufactured test vehicles. The consensus of the project team was that immersion silver has the best balance of desirable properties: good wetting by solders, good solder joint reliability, good long-term solderability upon storage, and retention of solderability after multiple reflow cycles. In addition, several major electronic manufacturing companies are currently using immersion silver in production.

Components

Components were selected to represent those commonly found on legacy military systems as well as new emerging technologies. Both plated through hole and surface mount component technologies were selected.

The team identified ten different component styles of high interest, of which the following eight types were ultimately included on the test vehicle: ceramic leadless chip carriers (CLCC), plastic leaded chip carriers

(PLCC), thin small outline packages (TSOP), thin quad flat packs (TQFP), ball grid arrays (BGA), plastic dual inline packages (PDIP), chip resistors, and chip capacitors.

Components and their Associated Lead Finishes

Component Type	Component Finish					
	SnPb	Sn	SnCu	SnAgCu	NiPdAu	SnAuCuBi
CLCC-20	X			X		X
PLCC-20		X				
TSOP-50	X		X			
TQFP-144		X				
TQFP-208					X	
BGA-225	X			X		
PDIP-20		X			X	
0402, 0805, & 1206 Capacitors		X				
1206 Resistors		X				

Pd = Palladium; Au = Gold

Board Design

The size of each test vehicle is 14.5"x 9" x0.092" and includes six layers. The manufactured boards were made from a laminate with a glass transition temperature (Tg) of ~170°C. Printed wiring assemblies designated as rework boards were made from a laminate with a glass transition temperature (Tg) of ~140°C. The board finishes selected for the test vehicles were: immersion silver for the lead-free printed wiring assemblies and SnPb hot air solder leveling (HASL) for the rework PWAs and the control PWAs.

Completed Test Vehicle

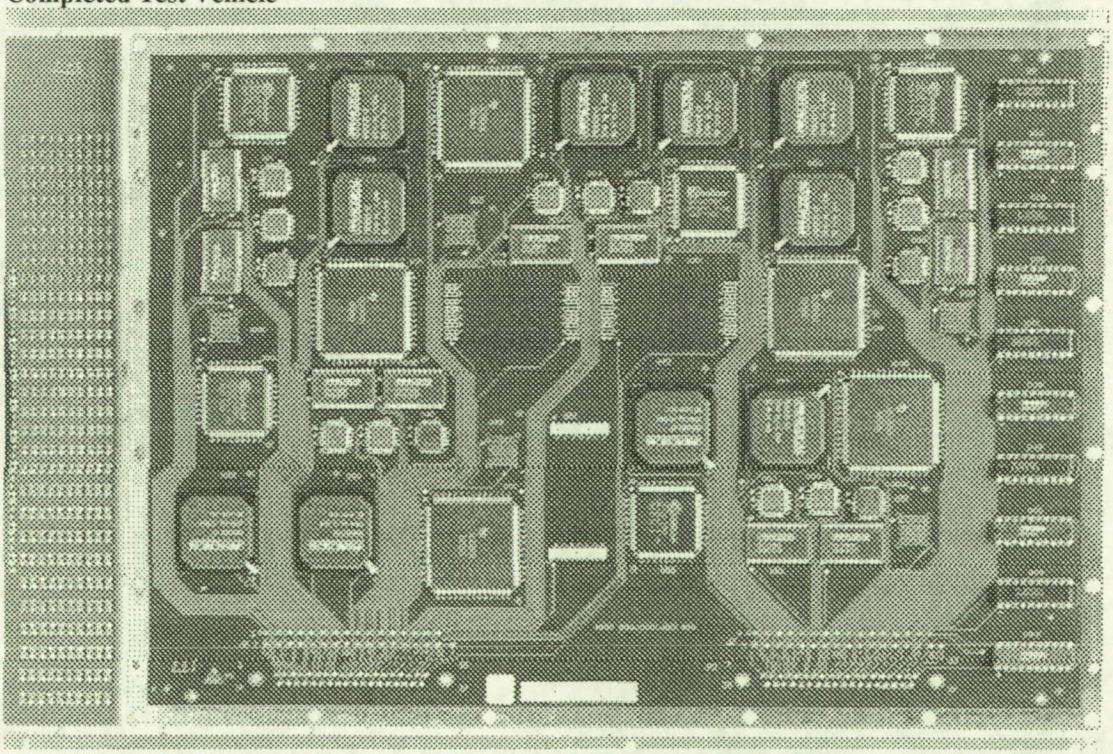


Photo Provided by Ms. Lety Campuzano-Contreras, BAE Systems Irving, Texas

To provide statistical validity, five test vehicles will be used in every test, with each vehicle containing at least five components of each type for a total of at least 25 components of each component type being subjected to testing. The complete testing program requires approximately 200 test vehicles. According to IPC guidelines, the completed test vehicle is categorized as a Type I assembly. Type I Assemblies are circuit boards with a combination of through hole devices and surface mount components on one side of board [5].

The circuit board was designed with daisy-chained pads that are complementary to the daisy chain in the components (except for the chip capacitors). Therefore, the solder joints on each component are part of a continuous electrical pathway that will be monitored during testing by an event detector (Anatech or equivalent). To eliminate premature failures that could be caused by vias and plated-through holes, each component has its own distinct pathway (channel) traced on the top surface of the board. Failure of a solder joint on a component during testing will break the continuous electrical pathway and be recorded as an event.

The components were not placed on the board in any actual product hardware configuration. Rather, they were grouped on the PWA as a block set, which was then replicated to various locations on the test vehicle.

One of the short ends of the test vehicle is a breakaway coupon containing all the resistors and capacitors. This design feature allows groups of capacitors and resistors to be removed from testing for analysis at regular interval during thermal cycling.

Assembly Process [6]

BAE Systems (Irving, Texas) (formerly Boeing Commercial Electronics) performed all the test board assembly with the exception of the lead-free wave soldering, which was performed by Vitronics-Soltec (Stratham, New Hampshire). BAE's facility was considered typical of one producing a highly reliable product with enough volume to simulate a higher capacity production run.

In general, the test vehicles were built using the same practices and procedures that BAE Systems Irving uses on a daily basis to assemble PWA's. For example, a 12 zone forced convection oven without inerting was used for both lead and lead-free reflow. Solder paste was placed onto the boards prior to assembly using a standard stencil printing process. The differences between lead and lead-free assembly were in the temperature profiles used during reflow and wave soldering. The lead-free assembly required both higher wave soldering pot temperatures and higher reflow oven temperatures and longer exposure times.

The flux systems used during soldering were "low residue" or no-clean fluxes and the group chose to clean the test vehicles after processing even though no-clean fluxes were used with some solder. Additionally, reflow was accomplished without nitrogen inerting, which might have created a smaller soldering process window (a credit to the BAE Systems crew for creating a quality test vehicle under such tough process conditions).

Solder Alloys and Associated Flux

Solder Alloy	Flux		
	Wave Soldering	**Reflow Soldering**	**Manual Soldering**
SnCu	VOC Free No Clean Flux	N/A	R Heat Stabilized Resin ROL0 Tacky Flux
SnAgCu	VOC Free No Clean Flux	ROL1	R Heat Stabilized Resin ROL0 Tacky Flux
SnAgCuBi	N/A	No Clean (RMA)	R Heat Stabilized Resin ROL0 Tacky Flux
SnPb	Type ORM0	ROL0	ORL0 ROL0 Tacky Flux

Table provided by BAE System Irving, Texas [6]
N/A = Due to limitations on board numbers and components, these solder alloys were not used during the noted assembly processes.
R = Rosin Base [7]
ROL0 = Rosin, Low or no flux/flux residue activity, no halide present [7]
ROL1 = Rosin, Low or no flux/flux residue activity, halide present [7]
ORM0 = Organic, Moderate flux/flux residue activity, no halide present [7]

Rework Procedures [6]

Components were removed and replaced on approximately one-third of the test vehicles. These reworked assemblies are undergoing the same testing as the newly manufactured test vehicles. The four component types that were reworked were the BGA's, the TQFP-208's , the TSOP's, the and PDIP's. Two of each component type were reworked on each rework test vehicle.

The rework performed was lead-free rework of tin-lead assemblies. This scenario represents the more imminent concern to military depots in the U.S. because of the possibility of servicemen unknowingly repairing a legacy SnPb circuit card in the field using lead-free solder. As such, the reason for including repair boards in the test program is to determine if mixing lead-free and a SnPb solder on the same PWA *has an adverse effect on part reliability. Lead-free rework was accomplished using the Sn3.9Ag0.6Cu,* Sn/0.7Cu.05Ni and Sn3.4Ag1Cu3.3Bi alloys in wire form. Tin/lead assemblies reworked using tin/lead solder is the experimental control. BAE Systems fully documented the test vehicle build process from start to finish.

Test Plan

The first step in developing the test plan was to review the performance requirements called out in applicable military and industry standards, and then select test methods recognized and agreed upon by the technical team members. A key factor was selecting test parameters that would subject enough environmental stress to cause solder joints to fail, thus permitting differentiation between lead vs. lead-free performance. Military document MIL-STD-810F and industry documents IPC-SM-785 and IPC-TM-650 were primary references used for writing the test plan. One test—the combined environments test—followed a procedure developed and used by Raytheon. In all, the team identified a total of nine environmental exposure and physical reliability tests.

In all cases, the team agreed that acceptable performance of a lead-free solder alloy means performance better than or equal to the eutectic tin-lead solder, in terms of fewer electrical failures. Failure of a test board in a specific test does not necessarily disqualify a lead-free solder alloy for use in an application for which that test does not apply.

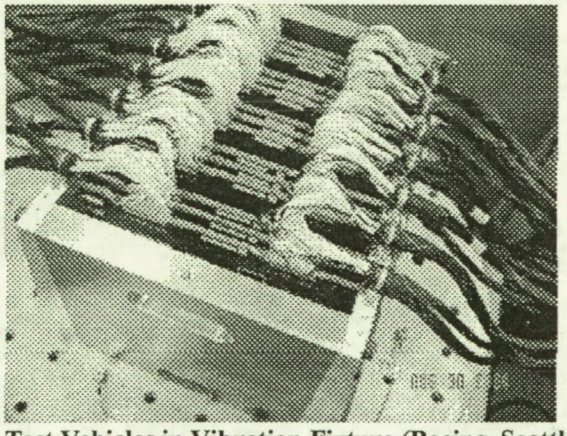
Common Tests

Five of the nine tests were agreed upon as necessary by virtually all of the team members and therefore deemed "common" tests. Both manufactured and reworked test vehicles will be subjected to all common tests.

Vibration

The vibration test determines solder joint failures during exposure to vibration conditions. The stakeholders agreed that MIL-STD-810F, Method 514.5 (Vibration), would be the stating point for developing a vibration test that would determine the reliability of the various solder alloys under severe vibration. Specific details on the vibration test can be found in the Joint Test Protocol, "*Joint Test Protocol, J-01-EM-026-P1, for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies*"; February 14, 2003 (Revised April 2004).

The vibration test will be run using vibration spectra created specifically for this project by the Electronic, Electrical and Electromechanical (EEE) Parts and Packaging Group of NASA Marshall Space Flight Center (MSFC). The test vehicles will be exposed to an initial 9.9 g_{rms} vibration spectrum in each of the three orthogonal axes for one hour per axis. After completion of the above, the Z-axis vibration level (perpendicular to the plane of the board) will be increased in 2.0 g_{rms} increments, shaking for one hour per increment until all parts fail, or the test is terminated. It is probable that most failures will occur during the vibration in the Z-axis because that is the axis that causes the most board bending.



Test Vehicles in Vibration Fixture (Boeing, Seattle, Washington)

Mechanical Shock

The purpose of the mechanical shock test is to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by rough handling, transportation, or field operation. Specific details on the mechanical shock test can be found in the Joint Test Protocol, "*Joint Test Protocol, J-01-EM-026-P1, for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies*"; February 14, 2003 (Revised April 2004).

Two consecutive mechanical shock tests will be conducted using two different methods based on MIL-STD-810F, Test Method 516.5. This procedure was selected because it addresses the exact requirements that many military customers must satisfy. Three shock transients will be applied in each direction along

each of the three orthogonal test vehicle axes. This test will be conducted using the following MIL-STD-810F shock response spectra, in sequence:

- Functional Test for Flight Equipment
- Functional Test for Ground Equipment
- Crash Hazard Test for Ground Equipment

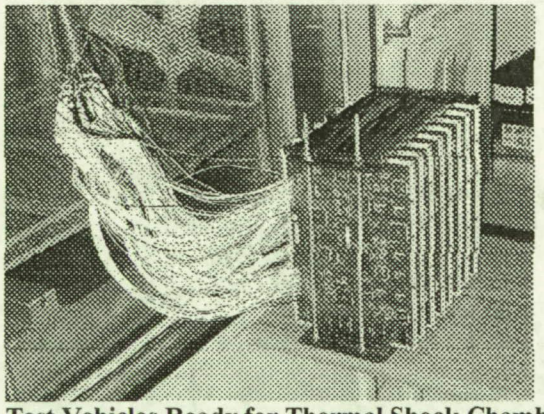
Following completion of the above, the test vehicles will be exposed to 100 shock transients in each direction along each of the three orthogonal axes using the Crash Hazard Test for Ground Equipment spectrum.

The second mechanical shock test that will be conducted partially follows Method 516.5, but calls for higher shock amplitudes (g's). The purpose of this test set is to provide a much harsher mechanical shock than Method 516.6. Shock transients will be applied 100 times only in the Z-axis only (normal to the plane of the board) for each of the following spectra in sequence: Functional Test for Flight Equipment, Functional Test for Ground Equipment and Crash Hazard Test for Ground Equipment. Then, the g levels will be increased step-wise in the Z-direction until failure of a majority of components is observed.

Running two test sets—one in all axes but using fewer shocks and smaller amplitudes, and the other in one axis using a higher number of shocks and increased amplitudes—will ensure that a wider range of test conditions will be covered. Furthermore, the second set of mechanical shock conditions will increase the likelihood that significant component failures will be achieved, allowing for better discrimination in alloy performance.

Thermal Shock

The thermal shock test determines a solder's resistance to extremely rapid changes in temperature. This test will be performed in accordance with MIL-STD-810F, Method 503.4, Procedure I (Temperature Shock Steady State). Specific details on the thermal shock test can be found in the Joint Test Protocol [2]. The test vehicles will be cycled between two chambers (hot/cold) held at -55°C and +125°C respectively for 1000 cycles while the electrical continuity of the solder joints is continuously monitored.



Test Vehicles Ready for Thermal Shock Chamber (Boeing, Seattle, Washington)

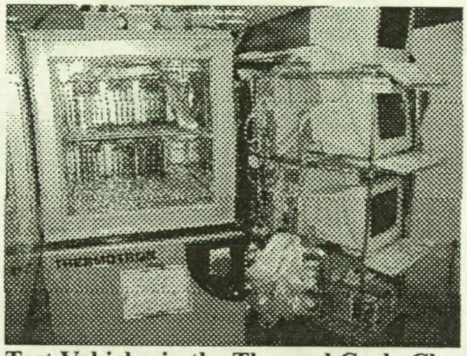
Thermal Cycling

The thermal cycle testing determines a solder's capability to withstand extreme thermal cycling. This test will be performed in accordance with IPC-SM-785 *(Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments)*.

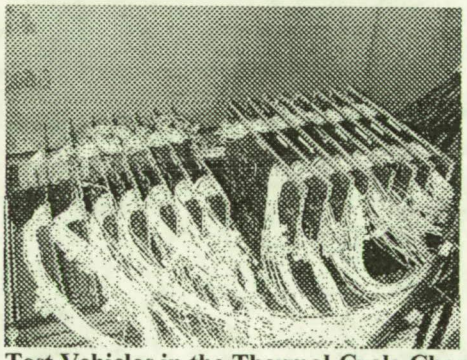
Thermal cycling will be conducted at two different conditions, -55 to +125°C and -20 to +80°C, Technical representatives from the U.S. Army Aviation and Missile Command (AMCOM) suggested two temperature ranges to allow for acceleration factors to be determined, which will permit extrapolation of the data to their systems' actual use conditions. The thermal cycle tests will be run until a significant number (greater

than 63 percent) of component failures is achieved in order to provide statistically meaningful data. Specific details on the thermal cycle test can be found in the Joint Test Protocol, "*Joint Test Protocol, J-01-EM-026-P1, for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies*"; February 14, 2003 (Revised April 2004).

A high-temperature dwell time of 30 minutes was chosen for both thermal cycling tests. Recent research publications suggest that dwell times longer than the standard 10 to 15 minutes are required because lead-free solders creep much slower than tin/lead solder. Since creep is a large contributor to solder damage, it is desirable to allow all of the solder under test to creep as much as possible in order to get a more realistic comparison between tin/lead solder and the lead-free solders. The low-temperature dwell time chosen was 10 minutes because little creep occurs at low temperatures and therefore the low temperature dwell is believed to be less important that the high temperature dwell.



Test Vehicles in the Thermal Cycle Chamber (Rockwell Collins, Cedar Rapids, Iowa)



Test Vehicles in the Thermal Cycle Chamber (Boeing, Seattle Washington)

Combined Environments Test

The combined environments test (CET) determines the reliability of solders under combined thermal cycle and vibration. The CET for the lead-free solder project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process. The project stakeholders felt that the CET would provide a quick method to identify comparative potential reliability differences in the test alloys vs. the Sn/Pb baseline. The primary accelerated environments are temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom used in combination). Specific details on the combined environments test can be found in the Joint Test Protocol, "*Joint Test Protocol, J-01-EM-026-P1, for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies*"; February 14, 2003 (Revised April 2004).

This test is performed utilizing a temperature range of –55 to 125°C with 20°C/minute ramps. The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-minute soak. A 10 g_{rms} pseudo-random vibration is applied for the last 10 minutes of the cold and hot soaks. Testing is

continued until sufficient data is generated to obtain statistically significant Weibull plots indicating relative solder joint reliability. If significant failure rates are not evidenced after 100 cycles, the vibration levels are incremented by 5 g_{rms} and cycling is continued for an additional 100 cycles. This process is repeated until all parts failed or 20 g_{rms} is reached.

Extended Tests

There are four extended tests: salt fog, humidity, surface insulation resistance, and electrochemical migration resistance. These tests supplement the common tests and were identified as system requirements by a subset of the team. For two of the extended tests, humidity and salt fog, the test vehicles are the same as those used for the common tests. However, for the surface insulation resistance and electrochemical migration test standard IPC test boards will be used.

Salt Fog

The salt fog test determines the effects of salt spray on the physical appearance of lead-free solder joints. Technical representatives from the Air Force F-15 program and Naval Air Warfare Center Weapons Division (NAWCWD) require MIL-STD-810F Method 509.4 (Salt Fog) (or equivalent) because this test simulates the coastal atmosphere to which U.S. Air Force and Navy aircraft are subjected. The salt fog test determines the resistance of the solders to a corrosive environment.

Humidity

The humidity test determines a test specimen's resistance to the deteriorative effects of high humidity and heat conditions. Technical representatives from the Air Force F-15 program and NAWCWD require MIL-STD-810F Method 507.4 (Humidity) (or equivalent) to evaluate, in an accelerated manner, the effect of high humidity and high temperature environments (i.e., tropical environment) on the lead-free solder joint function and appearance.

Surface Insulation Resistance (SIR)

The SIR test quantifies the effects of flux residues upon the electrical insulation resistance of the test vehicle. Technical representatives from NAWCWD require SIR testing to demonstrate the relative degree to which the lead-free test vehicle is susceptible to resistance decreases under high humidity and temperature conditions.

This test will be performed in accordance with IPC-TM-650, Method 2.6.3.3 (Surface Insulation Resistance, Fluxes). The test vehicle for SIR is a standard IPC-B-24 test coupon which was processed through the same soldering processes as the completed test vehicles. A list of the solder alloy/flux combinations being tested can be found in the Joint Test Protocol [2].

Electrochemical Migration Resistance (EMR) Test

The EMR test is used to provide a means to assess surface electrochemical migration on the lead-free solder test vehicles. Technical representatives from NAWCWD felt that electrochemical formation of metallic dendrites is a possible failure mode with any new alloy/flux combination.

This test will be performed in accordance with IPC-TM-650, Method 2.6.14.1 (Electrochemical Migration Resistance Test). The test vehicle for EMR is a standard IPC-B-25A "D-comb pattern" test coupon, which was processed through the same soldering processes as the completed test vehicles. A list of the solder alloy/flux combinations being tested can be found in the Joint Test Protocol [2].

Solder Joint Analysis

In conjunction with reliability testing, two other evaluations—lead-residue testing and cross-sectioning—will be performed. Both of these tests will allow for an analysis of the metallurgical properties of the solder joints. Testing will be conducted on solder joints following the completion of testing as well as on solder joints that were not exposed to testing conditions. For those solder joints that underwent testing, both failed and non-failed solder joints will be examined.

The lead residue test will serve to quantify lead residue in reworked test PWAs. This test involves the analysis of the amount of lead (Pb) remaining in the solder joints from reworked components. The testing will be a post-PWA-assembly test to quantify the amount of Pb remaining in the solder joint following rework. This test will help determine if Pb has an effect on lead-free joint reliability.

Cross-sectioning of the solder joints will determine which intermetallics are present and their location within the solder joints and the degree of crack formation within the solder joints.

Summary

The focus of the JCAA/JG-PP Lead-Free Solder Project is to quantify the reliability of lead-free solders compared to eutectic tin/lead solder. The test vehicles designed for this project are representative of those used on current defense and space systems. Solders validated by this project will have the potential to be transitioned for use on new program hardware, in OEM processes, and at depot and field-level facilities. This project brought together defense contractors and representatives from the affected military systems and depots. The stakeholders selected solder alloys, created a test protocol, and will analyze the test results to determine if the candidate lead-free alloys are suitable for implementation. In short, this test program was designed with the intent to provide practical, "real-life" technical data to allow solid decisions to be made about lead-free solders in the near future.

The lead-free solder project test methodologies will answer many questions about the suitability of lead-free solders for aerospace/military applications. Data generated from the testing program will provide an excellent test requirement template for OEM/customer discussion on how current tin-lead solder processes compare to lead-free solder processes. Test results from the project will eliminate the need for some product testing and allow resources to be expended on program specific or program unique test requirements.

For additional information on the JCAA/JG-PP Lead-Free Solder Project, visit the JG-PP Web site at www.jgpp.com .

Acknowledgments

The JG-PP/JCAA Lead-Free Solder Project acknowledges the following organizations for their contributions (many of which are in-kind) in helping develop the test program, in general, and the other specific activities noted below:

Rockwell Collins (notably Dave Hillman) for design of the test vehicle, procurement of testing materials, characterization of parts, and thermal cycle testing

BAE Systems (notably Lety Campuzano-Contreras) for conducting the assembly and rework of the test vehicles

Boeing — Tom Woodrow, for conducting vibration, thermal shock and thermal cycle testing, and John Kerr for providing the SIR and EMR test coupons as well as conducting SIR and EMR testing

NASA, Marshall Space Flight Center (notably Jim Blanche) for helping design the vibration test

American Competitiveness Institute (Lee Whiteman) for performing mechanical shock, salt fog, humidity, and lead-residue tests

NASA, Jet Propulsion Lab (notably Reza Ghaffarian) for helping design the mechanical shock test

Raytheon (Joe Felty and Jeff Bradford) for conducting combined environments testing

Sandia National Laboratories (Paul Vianco) for offering to perform cross-sectioning

U.S. Army Research, Development and Engineering Command (notably Dave Locker) for offering to perform data analysis and modeling

Heraeus, Senju Solder, Vitronics-Soltec, and Cirtech for donating solders for testing

CALCE (notably Mike Osterman) for offering to perform data analysis and modeling

Vitronics-Soltec for conducting lead-free wave soldering processes

Texas Instruments for providing components

Kyzen Corporation for cleaning the completed test boards following wave soldering processes

Corfin Industries for component tinning processes

References

[1] IPC-6011, "Generic Performance Specification for Printed Boards," *IPC Standards and Publications*, July 1996

[2] Joint Test Protocol, "*Joint Test Protocol, J-01-EM-026-P1, for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies*"; February 14, 2003 (Revised April 2004).

[3] Potential Alternatives Report, "*Potential Alternatives Report for Validation of Alternatives to Eutectic Tin-Lead Solders used in Electronics Manufacturing and Repair*"; August 4, 2003 (Revised September 23, 2003).

[4] IPC/EIA J-STD-006A, "Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications," *EIA and IPC Standards and Publications*, May 2001

[5] IPC-2222, "Sectional Design Standard for Rigid Organic Printed Boards," *IPC Standards and Publications*, February 1998

[6] Campuzano-Contreras, Lety, "Status Report on Assembly of Lead-Free Project Test Boards," *Presented at the September 21 Lead-Free Solder Project Meeting, Melbourne, Florida,* September 21, 2004

[7] IPC J-STD-004A, "Joint Industry Standards; Requirements for Soldering Fluxes"

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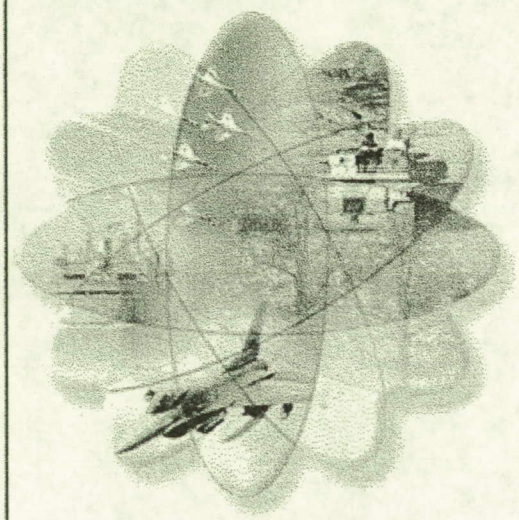

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****Joint Service Solvent Substitution Tracking System ** *New!!***

This site last updated October 31, 2004.

Send all questions and comments to jgpp@ctc.com

Chan, Melanie R

From: Brown, Christina M
Sent: Tuesday, November 30, 2004 10:01 AM
To: Chan, Melanie R
Subject: *FW: LFS Article*

Melanie: I hope you had a great Thanksgiving. Attached is an article that is proposed for publishing and distribution within the electronics community by ACI (See info below). My office is the primary NASA participant in this NASA/DoD Joint Project. The article provides a status of project activities to date and is being staffed to all membersof the project consortia. One of the premises of these joint projects is that all information is public (no proprietary data is included) and as such I haven't had any Export Control issues in the past but I like to keep the appropriate parties in the loop. Are you still responsible for YA Export Control issues? If not, do you know who I should run this by. The project team is looking for my concurrence to release the article. Give me a call if you have any questions. Thanks

Christina M. Brown
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Background:

The American Competitiveness Institute (ACI) operates the Electronics Manufacturing Productivity Facility (EMPF), which serves as the National Electronics Manufacturing Center of Excellence. The EMPF is considered as an authority in electronics manufacturing and electronics use in the Navy. The EMPF can help define, perfect, and certify the Lead Free Soldering processes which the Navy will accept such that when implemented within an aerospace and military electronics manufacturer's facility, it will be considered as an accepted practice for use to develop naval platform electronic systems.

ACI actively participates in several Lead Free Soldering technical consortiums. Among the consortiums are:

- Lead Free Components Focus Group
- JG-PP Lead Free Soldering Program
- University of Maryland's Computer Aided Life Cycle Engineering (CALCE) Electronic Products and Systems Center
- Aerospace Industries Association Lead-free Aerospace Electronics Working Group (AIA LAEWG)

To better serve the electronics manufacturing community, ACI is initiating a Lead Free Soldering Journal. The goal is to provide a written forum on the current state of the art of Lead Free Soldering. The customer (reader) will be anyone who is interested in applying Lead Free solders to a production environment. The journal's focus should not be limited to aerospace and military applications.