Fabrication of Silicon Backshorts with Improved Out-of-Band Rejection for Waveguide-Coupled Superconducting Detectors

E. Crowe[1], C.L. Bennett[2], D.T. Chuss[1], K.L. Denis[1], J. Eimer[3], N. Lourie[1], T. Marriage[2], S.H. Moseley[1], K. Rostem[1], T.R. Stevenson[1], D. Towner[1], K. U-Yen[1], E.J. Wollack[1]

[1]NASA / GSFC, Greenbelt, MD, USA,

[2]Johns Hopkins University Department of Physics and Astronomy, Baltimore, MD, USA,

[3]Johns Hopkins University Department of Physics and Astronomy, Greenbelt, MD, USA.

Detector Fabrication Process

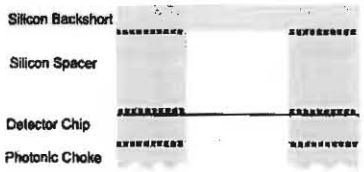
Silicon on Insulator (SOI) wafer: Deposit Nb ground plane and polymer layer for wafer bonding

Bond to a low resistivity wafer which will function as an integrated silicon waveguide

Remove the SOI handle layer and buried oxide. The 5um SOI device layer functions as the OMT membrane,TES thermal isolation membrane and microstrip dielectric.

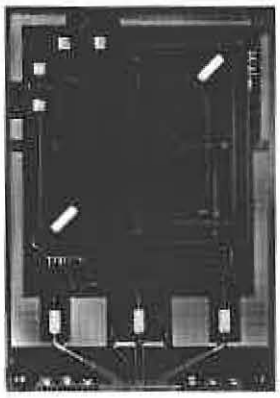
Complete MoAu TES, niobium microstrip, and silicon thermal isolation processing on the device layer side

Temporary bond to pyrex wafer(not shown) and deep reactive ion etch (DRIE) to define OMT and release silicon thermal isolation membranes

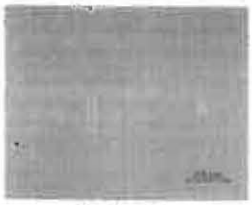


Indium bump bond separately fabricated silicon spacer and silicon backshort chip as well as silicon photonic choke chip.

40 GHz Detector

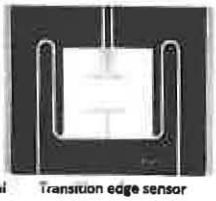


Magic-T combines out of phase signal component and terminates in-phase signal

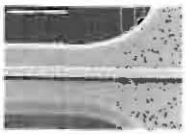


On chip filtering

Si membrane for thermal conductance control

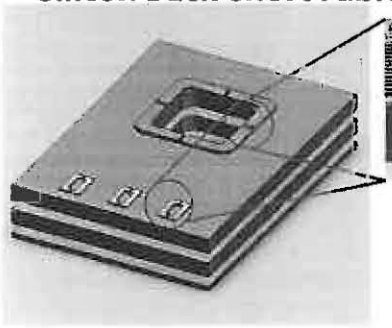


Transition edge sensor

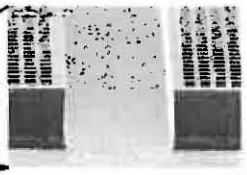


Silicon teather with Nb microstrip

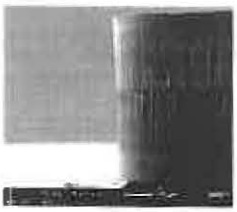
Silicon Back-short Fabrication and Integration



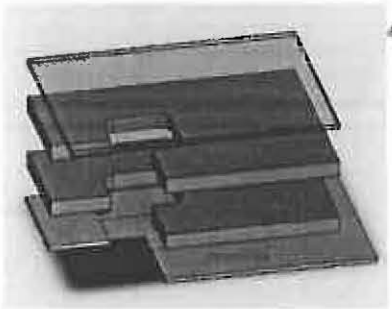
Backshort assembly



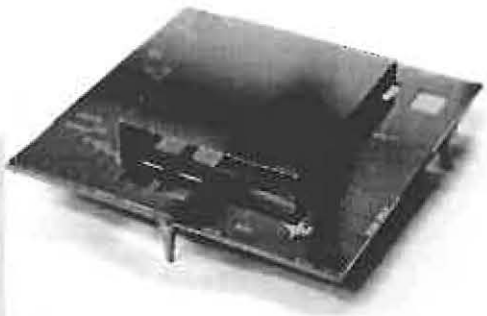
Mouse hole for microstrip isolates OMT and TES membranes



Silicon sidewall profile etched by DRIE



Backshort integration to detector chip



Detector integrated with backshort