voltage/current and only needs power to change states (i.e., on and off). Furthermore, no power is required to maintain the states; hence, the state of the switch is nonvolatile. Because of these attributes the integration of a rectenna to provide the necessary power and control is unique to this embodiment. A rectenna, or rectifying antenna, generates DC power from an incident RF signal. The low voltages and power required for the nanoionic switch control are easily generated from this system and provide the switch with a novel capability to be operated and powered from an external wireless device. In one realization, an RF signal of a specific frequency can be used to set the switch into an off state, while another frequency can be used to set the switch to an on state.

The wireless, miniaturized, and nomoving-part features of this switch make it suitable for applications such as integration into garments, RFID (radio-frequency identification) tags, and conformal structures (e.g., aircraft wings, sounding rockets contours, etc). In the case of RFID tags the innovation will provide countermeasures to attempts for identity theft and other uninvited attempts for retrieval of information. It could also be applicable to the automotive industry as well as the aerospace industry for collision avoidance and phased array radar systems, respectively.

This work was done by James Nessel and Felix Miranda of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18919-1.

Compute Element and Interface Box for the Hazard Detection System

This architecture combines an FPGA and CPU to capitalize on their strengths.

NASA's Jet Propulsion Laboratory, Pasadena, California

The Autonomous Landing and Hazard Avoidance Technology (ALHAT) program is building a sensor that enables a spacecraft to evaluate autonomously a potential landing area to generate a list of hazardous and safe landing sites. It will also provide navigation inputs relative to those safe sites.

The Hazard Detection System Compute Element (HDS-CE) box combines a field-programmable gate array (FPGA) board for sensor integration and timing, with a multicore computer board for processing. The FPGA does system-level timing and data aggregation, and acts as a go-between, removing the real-time requirements from the processor and labeling events with a high resolution time. The processor manages the behavior of the system, controls the instruments connected to the HDS-CE, and services the "heavy lifting" computational requirements for analyzing the potential landing spots.

The HDS-CE is built with commercial off-the-shelf (COTS) components and one custom I/O board. The HDS consists of the compute element, a Flash LIDAR, a 2-axis gimbal, a navigation-grade inertial measurement unit (IMU), and a power distribution unit (PDU). It is designed as an independent instrument interfacing with a host vehicle.

This architecture combines the strengths of two architectures: the high-performance timing, I/O, and interface ability and processing of an FPGA, with the high-performance computing, flexi-



The ALHAT Hazard Detection System Compute Element.

bility, and programmability of a generalpurpose Manycore processor. This combination of an FPGA with a Manycore processor, with both components being concurrently used for processing, has yet to be done for space applications.

This architecture is also useful for embedded robotic applications such as rovers. The FPGA/Manycore combination allows the end user to place tasks on either the FPGA or the Manycore processor, based on the strengths and weaknesses of each component.

This work was done by Carlos Y. Villalpando, Garen Khanoyan, Ryan A. Stern, Raphael R. Some, Erik S. Bailey, John M. Carson, Geoffrey M. Vaughan, Robert A. Werner, Phil M. Salomon, Keith E. Martin, Matthew D. Spaulding, Michael E. Luna, Shui H. Motaghedi, Nikolas Trawny, Andrew E. Johnson, Tonislav I. Ivanov, Andres Huertas, and William D. Whitaker of Caltech; and Steven B. Goldberg of Indelible Systems, Inc. for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

The software used in this innovation is available for commercial licensing. Please contact Dan Broderick at Daniel.F.Broderick@jpl.nasa.gov. Refer to NPO-48786.

🗢 DOT Transmit Module

NASA's Jet Propulsion Laboratory, Pasadena, California

The Deep Space Optical Terminal (DOT) transmit module demonstrates the DOT downlink signaling in a flight electronics assembly that can be qualified for deep space. The assembly has the capability to generate an electronic pulse-position modulation (PPM) waveform suitable for driving a laser assembly to produce the optical downlink signal. The downlink data enters the assembly through a serializer/ deserializer (SERDES) interface, and is encoded using a serially concatenated PPM (SCPPM) forward error correction code. The encoded data is modulated using PPM with an inter-symbol guard time to aid in receiver synchronization. Monitor and control of the assembly is via a low-voltage differential signal (LVDS) interface.

This work was done by Kevin J. Quirk, Jonathan W. Gin, Adit Sahasrabudhe, Ferze D. Patawaran, Danh H. Nguyen, and Huy Nguyen for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-47723