



An Automated Safe-to-Mate (ASTM) Tester

This tester allows for fast, safe, and reliable checkout of connector interfaces for both critical flight hardware and companion ground support equipment (GSE).

Goddard Space Flight Center, Greenbelt, Maryland

Safe-to-mate testing is a common hardware safety practice where impedance measurements are made on unpowered hardware to verify isolation, continuity, or impedance between pins of an interface connector. Performing this on critical flight hardware under test and its associated GSE ensures minimal risk when the hardware is powered. Historically, safe-to-mate measurements are performed manually with data written into paper procedures. This laborious process potentially requires a large amount of time for connectors that could have as many as 104 pins. Risks include human error in performing the measurements on sensitive inputs or in recording the data as well as potential loss of hardcopy data.

A computer-based instrumentation solution has been developed to resolve all of these issues. The ASTM is connected to the circuit under test, and can then quickly, safely, and reliably safe-to-mate the entire connector, or even multiple connectors, at the same time. The operation is completely automated, so that personnel can devote time to other tasks. When the automated safe-to-mate is finished, data is retained as electronic

records that can be saved for later review.

The ASTM marries off-the-shelf modular components such as a computer, multiplexers, and a digital multimeter (DMM) with a custom printed circuit board all in a chassis. This approach enables multiple, identical, automated safe-to-mate units to be constructed. Test engineers will not have to worry about finding and using the same DMM as the last time, as all of the units will contain an identical model. Safety has also been designed into this system by purposely selecting a DMM that outputs a very low voltage and current to make the measurements. A resistor has also been placed in parallel with the load being measured to further limit the current output of the digital voltmeter.

The ASTM software can read in schematic netlists from common tools such as Orcad or Mentor Graphics DXDesigner and can automatically determine the type of measurements. For example, it can determine which pins should be shorted together (e.g., power connections or ground connections), and will test that they are indeed shorted. The program also has a learning function that allows it to make im-

pedance readings for those cases where a design netlist is not available (i.e., the hardware is essentially treated as a black box). Finally, the software saves all data into a file that it can use in the future to verify that the board does not change, or that identical boards that should have the same impedances actually do.

The system can handle pins with capacitive and diode loads. For example, the software senses the charge-up effect characteristic of capacitors to know that the load is capacitive. Finally, the ASTM employs a custom printed circuit board to handle the routing of signals between its front I/O connectors and its internal instrumentation multiplexers. This makes the system more reliable than other units that employ large, custom, internal harnesses. This also greatly reduces the size and the cost of assembly. Users simply develop test harnesses between the ASTM and their hardware under test.

This work was done by Phuc Nguyen, Michelle Scott, Alan Leung, and Michael Lin of Goddard Space Flight Center; and Thomas Johnson of Microtel LLC. Further information is contained in a TSP (see page 1). GSC-16098-1

Wireless Chalcogenide Nanoionic-Based Radio-Frequency Switch

The integration of a rectenna makes it possible to wirelessly control the nanoionic switch completely without onboard power.

John H. Glenn Research Center, Cleveland, Ohio

A new nonvolatile nanoionic switch is powered and controlled through wireless radio-frequency (RF) transmission. A thin layer of chalcogenide glass doped with a metal ion, such as silver, comprises the operational portion of the switch. For the switch to function, an oxidizable electrode is made positive (anode) with respect to an opposing electrode (cathode) when sufficient

bias, typically on the order of a few tenths of a volt or more, is applied. This action causes the metal ions to flow toward the cathode through a coordinated hopping mechanism. At the cathode, a reduction reaction occurs to form a metal deposit. This metal deposit creates a conductive path that bridges the gap between electrodes to turn the switch on. Once this conductive path is formed,

no further power is required to maintain it. To reverse this process, the metal deposit is made positive with respect to the original oxidizable electrode, causing the dissolution of the metal bridge thereby turning the switch off. Once the metal deposit has been completely dissolved, the process self-terminates.

This switching process features the following attributes. It requires very little

voltage/current and only needs power to change states (i.e., on and off). Furthermore, no power is required to maintain the states; hence, the state of the switch is nonvolatile. Because of these attributes the integration of a rectenna to provide the necessary power and control is unique to this embodiment. A rectenna, or rectifying antenna, generates DC power from an incident RF signal. The low voltages and power required for the nanoionic switch control are easily generated from this system and provide the switch with a novel capability to be operated and powered from

an external wireless device. In one realization, an RF signal of a specific frequency can be used to set the switch into an off state, while another frequency can be used to set the switch to an on state.

The wireless, miniaturized, and no-moving-part features of this switch make it suitable for applications such as integration into garments, RFID (radio-frequency identification) tags, and conformal structures (e.g., aircraft wings, sounding rockets contours, etc). In the case of RFID tags the innovation will provide countermeasures to attempts for identity theft and other uninvited at-

tempts for retrieval of information. It could also be applicable to the automotive industry as well as the aerospace industry for collision avoidance and phased array radar systems, respectively.

This work was done by James Nessel and Felix Miranda of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18919-1.

Compute Element and Interface Box for the Hazard Detection System

This architecture combines an FPGA and CPU to capitalize on their strengths.

NASA's Jet Propulsion Laboratory, Pasadena, California

The Autonomous Landing and Hazard Avoidance Technology (ALHAT) program is building a sensor that enables a spacecraft to evaluate autonomously a potential landing area to generate a list of hazardous and safe landing sites. It will also provide navigation inputs relative to those safe sites.

The Hazard Detection System Compute Element (HDS-CE) box combines a field-programmable gate array (FPGA) board for sensor integration and timing, with a multicore computer board for processing. The FPGA does system-level timing and data aggregation, and acts as a go-between, removing the real-time requirements from the processor and labeling events with a high resolution time. The processor manages the behavior of the system, controls the instruments connected to the HDS-CE, and services the "heavy lifting" computational requirements for analyzing the potential landing spots.

The HDS-CE is built with commercial off-the-shelf (COTS) components and one custom I/O board. The HDS consists of the compute element, a Flash LIDAR, a 2-axis gimbal, a navigation-grade inertial measurement unit (IMU), and a power distribution unit (PDU). It is designed as an independent instrument interfacing with a host vehicle.

This architecture combines the strengths of two architectures: the high-performance timing, I/O, and interface ability and processing of an FPGA, with the high-performance computing, flexi-



The ALHAT Hazard Detection System Compute Element.