A Motor Drive Electronics Assembly for Mars Curiosity Rover: an Example of Assembly Qualification for Extreme Environments

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***Abstract* — This paper describes the technology development and infusion of a motor drive electronics assembly for Mars Curiosity Rover under space extreme environments. The technology evaluation and qualification as well as space qualification of the assembly are detailed and summarized. Because of the uncertainty of the technologies operating under the extreme space environments and that a high level reliability was required for this assembly application, both component and assembly board level qualifications were performed.**

Keywords – Assembly qualification, component qualification, qualification for extreme environments, extreme environment electronics and packaging, Mars rover

I. INTRODUCTION

For NASA Mars Curiosity Rover or Mars Science Laboratory (MSL), a motor drive electronics assembly was needed to be placed outside of the spacecraft and, therefore, was exposed to a radiation environment and a temperature range of -120°C to 125°C, which is beyond the military standard temperature range of -55ºC to 125ºC. A high level of reliability was required for this application. However, neither military nor commercial electronics nor packaging materials were designed for the environment. This challenge called for an application-specific assembly qualification approach for technology infusion and space application at an optimized combination of component level and assembly board level qualification processes. The design-for-reliability approach for the technology and the application-specific assembly qualification methodology for the space, developed for the electronics and assembly materials for the Mars Curiosity Rover, have provided the critical path for the technology infusion and mission success.

In this paper, the technology development and infusion of the motor drive electronics assembly, along with the technology and space qualification, is described. The process is an example of the qualification methodology for extreme environments and for assemblies when a high level of reliability is requires.

II. TECHNOLOGY DEVELOPMENT AND INFUSION

The electronics and packaging technologies have been evaluated for extreme environment applications for space missions [1-2]. The performance and reliability of the technologies are the major concern and challenge for the assembly under wide temperature range. Based on the technology evaluation, technology development effort was focused on an operational amplifier and the packaging materials for the assembly under the wide temperature space environment.

A. Electronics

A list of electronics for the motor drive electronics system was selected based on the design needs as well as potential survivability and reliability of the electronics technology, and encompassed a number of discrete transistors, capacitors, resistors, digital gates, mixed signal circuits, and operational amplifiers (op-amp).

A functional go/no-go testing on the electronics down to as low as -180°C was first conducted to characterize the electronics at low temperatures [3-4]. While the majority of the electronics selected were functional and survived the low temperature test, all the op-amps tested failed to meet the performance requirements of the assembly over the wide temperature range. Therefore, the technology development effort was focused on the design, fabrication and qualification of an op-amp to ensure performance, radiation and long term reliability requirements over the temperature range of -150°C to +125°C.

1) Design for performance:

The goal was to develop an op-amp that minimizes variation in key performance parameters over a wide temperature range of -150°C to 125°C.

Since it is desirable to simultaneously minimize variations in both small- and large-signal performance of the op-amp over the wide temperature range, a constant inversion coefficient (*IC*) current reference approach was developed, over either constant g_m bias optimum for minimizing variations in small-signal performance or constant current *I* bias optimal for minimizing the variations in the large-signal performance of the circuit [5].

Table 1 gives an example of slew rate and bandwidth ratios between -140°C and 85°C, and it is evident that the constant *IC* approach provides lower overall temperature dependence.

Table 1. Slew Rate and Bandwidth Temperature Dependence of 85°C to -140°C for the Three Bias Techniques

	Constant *I*	Constant g_m	Constant *IC*
SR Variation (SR_{85}/SR_{-140})	1	W.I.:2.7 S.I.: 4.4	1.64
BW Variation (BW_{85}/BW_{-140})	W.I.: 0.37 S.I.: 0.48	1	0.609

2) Design for reliability:

SOI technology was evaluated for the wide temperature applications [6] and to ensure rad-hardness, a certified 3.3V SOI process was chosen as the fabrication of the op-amp. However, the assembly was required to be a 5V board from the system perspective, and hence the op-amp needed to be 5V compatible. The 5V system level compatibility combined with reliability requirement complicated the design of the op-amp.

Extensive simulation was first used to analyze the operating bias conditions of the transistors under the worst case supply bias condition to determine that all voltage swing across all the terminals of the transistors were limited to about 3.5 V. Since the process had been qualified for a temperature range of -55°C to 125°C at 3.6V, the op-amp was expected to achieve its required reliability during this military temperature range if both V_{DS} and V_{GS} were smaller than 3.6V. In the case of excessive V_{DS}, cascade devices were added and for excess V_{GS}, the voltage level was clamped, shown in Figure 1 [5].

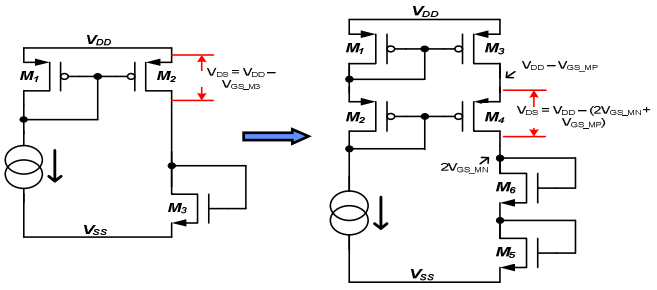

Figure 1. Cascading to reduce excessive V_{DS} across the device.

Since the operating temperature is wider than the military temperature range, design for hot carrier reliability approach was incorporated into the op-amp design to address the degradation or failure mechanisms at the lower temperature end, which is below -55°C. The design rules were developed as follows [7-8].

First, the hot carrier aging tests were performed on the 3.3V SOI NMOSFET and PMOSFET transistors with multiple channel lengths and widths under both maximum and non-maximum substrate current conditions at various temperatures down to -160ºC to understand the length/width effects, worst bias conditions and activation energy of the hot carrier aging for the process. Parametric characteristics were recorded during the hot carrier aging testing, including saturation current I_{dsat}, threshold voltage V_{th}, transconductance g_m, and drain conductance g_{DS}.

Second, sensitive analysis on the assembly circuit was performed and small-signal bandwidth was determined as the critical parameter for the op-amp in the design. While current drivability is the most significant device parameter for digital applications, which can be described by I_{dsat}, device differential parameters, such as transconductance g_m and drain conductance g_{ds}, are essential for analog applications, since the small-signal voltage gain, g_m/g_{ds}, is the maximum achievable single device amplification. Based on a single-ended output differential amplifier, the gain and offset voltage can be expressed as the function of transistor transconductance g_m, and furthermore, 10% g_{max} degradation was defined as the hot carrier aging failure criterion from the perspectives of assembly circuit performance, op-amp performance, as well as transistor reliability [7].

Third, the thermal profile of the op-amp was derived based on the power dissipation of the op-amp and the environmental temperature profile for the mission. The hot carrier lifetime for the op-amp was simulated and calculated based on the thermal profile rather than assuming a worst-case constant operating temperature to address the varying operating condition [8-9].

Fourth, a statistical approach was developed to extrapolate the op-amp reliability under the varying temperature range [5]. It was demonstrated that the statistical nature of transistor lifetime and the transistor bias distributions have great impact on circuit reliability. This statistical approach provided a more realistic circuit reliability project or estimation based on transistor lifetime distributions and transistor bias distributions.

Finally, the distribution of the hot carrier life time of the transistor, with the failure criterion determined by the op-amp performance on the assembly circuit earlier on, was then estimated as a function of transistor size. Furthermore, a minimum channel length was chosen for the op-amp design to achieve a targeted hot carrier mission life time with required margin under the mission thermal profile [7].

3) Radiation:

Generally speaking, SOI technologies have greatly reduced device susceptibility to SEE by simply truncating charge collection with an insulating oxide layer just below the active Si region, and largely eliminated Single Event Transients (SET) because the isolation of device wells removes any lateral parasitic paths. While the total ionizing dose level for this mission is relatively benign, high-energy heavy ions can still lead to Single Event Effects (SEE) such as analog transients on the op-amp. Previous studies in linear technologies amplifiers and comparators have shown them to be particularly susceptible to Analog SET [10-11].

Two types of devices were fabricated for the analogy SET investigation: one is a SLOW part with CrSiN thin-film resistors in place, and the other is a FAST part where these resistors had been removed from the circuit using a Focused Ion Beam. Spice simulations on an earlier design of the device concluded that several stages of the amplifier were likely to be

extremely sensitive to SET with voltage swings as high as the supply rail.

Broad beam high-energy heavy-ion tests were first performed. Transient signatures collected appeared to suggest a complex interaction involving a sensitive region initiating a response at other points in the circuit. The heavy-ion microbeam was then used to locate and confirm that the region of SET susceptibility was in the common bias circuitry of the op-amp. It was concluded that the op-amp, excluding the bias region, was to be largely insensitive to SET and was predicted to perform well for the mission.

The radiation evaluation required a design improvement in the bias circuitry, and a new design of the bias circuitry was integrated to mitigate the analog SET sensitivity for the flight op-amp.

B. Assembly Board

For survival of the assembly board in the low temperature and high fatigue environment, typical packaging materials and part finishes for commercial applications may not be used, and the assembly processes, such as die bonding and heavy aluminum wire bonding, need to be investigated and re-defined.

The assembly board for the evaluation was designed as a double-sided, high density board incorporating chip-on-board (COB) packaging technology. A couple of sets of commercially available material combinations with different manufacturing processes were selected based on its military and space flight heritage and material properties. Two rounds of experiments with test vehicles were designed using a full-factorial experimental design and 10 samples for each materials combination. The assembly boards were fabricated and visually inspected to JESD22-B101, and tested under thermal cycling of -120°C to +85°C with a ramp rate of 5°C/min and a dwell of 10 min at each extreme. The monitoring and data recording for electrical continuity was a continuous scan during the temperature cycling. Details of the selection process and assembly testing and analysis, including the design of the test vehicles, test set-up and continuous monitoring, detailed test results, wire bond modeling, failure analysis with SEM cross-section images, and some materials combination suggestions can be found in the references [3-4, 12-15]. This paper is focused on the qualification process for the technology development with the summary of the results.

1) Experiment one:

For experiment one, polyimide, alumina and Low Temperature Co-Fired ceramic (LTCC) were considered for substrates, while Ablebond 967-1, pure Indium and Zymet TC-611 were selected for die attach materials, and Hysol FP-4402, Hipec Q1-4939 and Parylene C were for encapsulant or overcoating materials. All wires used on the test vehicles during experiment one were 1 mil Au wire, which is 25.4 µm in diameter. Experiment one also included three different die sizes of bare silicon, along with through-hole and buried vias with 508 µm +/- 50.8 µm in diameter.

There was no evidence of vias failures or die or adhesive cracking for all die sizes tested during experiment one. The failure criterion was determined by at least greater than 10% of resistance increase occurred during the manual resistance measurements. Figures 2 shows the results of experiment one on the materials selection for substrate, die attach, encapsulant or overcoating, as function of the total number of thermal cycles surviving for each material combinations. The columns without red-outlines are for tests gone through these cycles without failures, while the columns with the red-outlines are for tests gone through the cycles with failures.

The six material combinations which survived at least 2000 thermal cycles during experiment one are cycled in Figure 2. All six material combinations involved polyimide or LTCC substrates, while none of the combinations on alumina substrates survived beyond 2000 cycles. The root cause of failure for the material combinations during experiment one was due to thermal stress on the wire bond from the overcoating material. FP4402 epoxy and Q1-4939 silicone were thicker encapsulants and, therefore, most likely resulted in higher thermal stress and lower fatigue life on the wire bonds.

From experiment one, it was indicated that: a) polyimide substrate with each of the three die attach materials and Parylene C yield the most promising results for the wide temperature survivability, and b) FP-4402 is promising overcoating choice when used with Ablebond 967-1 on LTCC substrate.

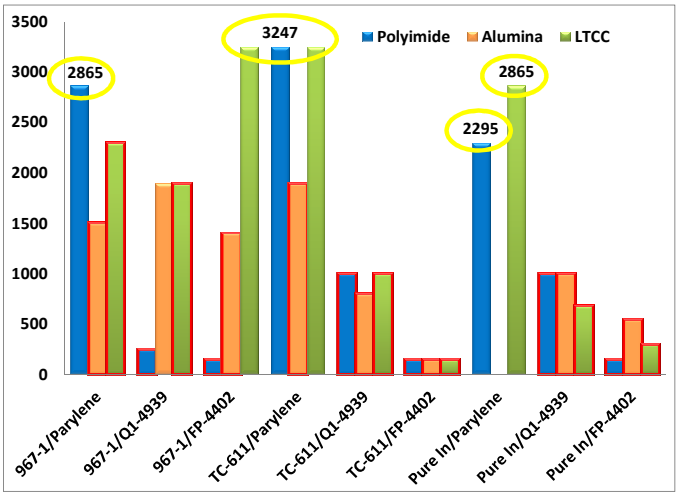

Figure 2. Summary of Experiment One: circled material conbinations survived over 2010 thermal cycles without failures.

2) Experiment two:

Experiment two was designed based on the surviving material combinations from experiment one with modifications and additions. Through-hole and buried vias were the same as experiment one. Q1-4939 and Parylene C

considered for overcoating materials. The summary and comparison of the material combinations for experiment one and two are provided in Table 2.

First, a power silicon MOSFET die with heavy aluminum wire bonds was included in the experiment. For the power MOSFET, an electrically and thermally conductive adhesive Zymet 6000.2 replaced Zymet TC-611 to address its packaging needs. In addition, an indium alloy $In_{80}Pb_{15}Ag_5$ replaced pure indium due to its better wetting capability and, therefore, an easier manufacturing process. Aluminum bond wires with 508 µm and 127 µm in diameter, respectively, were also considered for the power MOSFET.

Second, a 1506 resistor was included to address the size limit of passives and their encap finish. 1506 was assumed as the largest passive component size and the encap finish for the resistor were Ni/Au and Sn62Pb36Ag2.

Third, a 37-pin Nanonics Dualobe® connector (nano-connector) with surface mount BeCu lead attach was included with Sn63Pb37, In80Pb15Ag5, and Sn60Pb40 lead finish.

The same failure criterion was applied to experiment two. Also the same as experiment one, there was no vias failures or die or adhesive cracking for all die sizes tested.

Table 2. Summary and Comparison of Material Combinations for Experiment One and Two

	Experiment One	Experiment Two	
Substrate	Polyimide (Organic) Alumina/Al2O3 (Ceramic) Low Temperature Co-Fired Ceramic (LTCC) (Ceramic)	Polyimide (Organic) Low Temperature Co-Fired Ceramic (LTCC) (Ceramic)	
Die Attach	Ablebond 967-1 (Epoxy - silver-filled, electrically conductive adhesive) Pure Indium (Solder) Zymet TC-611 (Silicone based, thermally conductive adhesive)	1506 Resistor	Ablebond 967-1 (Epoxy) In80Pb15Ag5 (Solder)
		Power MOSFET	Ablebond 967-1 (Epoxy) In80Pb15Ag5 (Solder) Zymet 6000.2
Wire Type	Au 25.4 µm in diameter (99.9%)	Power MOSFET Heavy Al Wire	99.999% Al, 508 µm in diameter 99.99% Al, 127 µm in diameter
Die Size	Bare Silicon die 2.2 mm^2, 5 mm^2, 10 mm^2 with wire bonds 22 mm^2 x 22 mm^2 without wire bonds	1506 Resistor, power MOSFETs	
Encapsulant or Overcoating	Hysol FP-4402 (Epoxy) Hipec Q1-4939(Silicone) Parylene C (Polymer)	Hipec Q1-4939(Silicone) Parylene C (Polymer)	
Through-hole and Buried Vias	508 µm +/- 50.8 µm diameter Vias on Polyimide with a minimum Cu thickness of 25.4 µm Vias on thick-film alumina filled with Dupont Au 9591 or 5727 Vias on LTCC filled with thick-film Au, Kyrocera 30-065VM2	508 µm +/- 50.8 µm diameter Minimum Cu thickness of 25.4 µm	

Figures 3 shows the results of experiment two on the materials selection for substrate, die attach, encapsulant or overcoating, encap material and staking, wire diameter for MOSFET and nano-connector as function of the total number of thermal cycles surviving for each material combinations. Figure 4 shows the results for resistors. For both figures, the columns without red-outlines are for tests gone through these cycles without failures, while the columns with the red-outlines are for tests gone through the cycles with failures.

The seven material combinations for MOSFETs and nano-connectors which survived at least 2000 thermal cycles during experiment two are cycled in Figure 3.

All the Aluminum bond wire with 508 µm in diameter for the power MOSFETs failed. Aluminum bond wire with 217 µm in diameter survived with 6000.2 die attach and either Q1-4939 or Paralene C on both substrates. The failures of the heavy Al wire with 508 µm in diameter were due to thermal stress induced by the difference in coefficient of thermal expansion and change of temperature and manufacturing conditions [13-14]. For comparison of the two wires, the bonded region was small compared to the footprint of the wire bond foot on the pad, which yielded a lower strength bond under the wide temperature range.

2216 B/A appeared to be an optimal staking material to secure the nano-connector compared to the TC-611 because it was more rigid in preventing the connector shell from moving during flight vibration tests and mating/de-mating procedures. The staking material, however, did not seem to contribute to the nano-connector failure mechanism, which was a combination of a low fatigue life from brittle intermetallics and the brittle nature of tin at low temperature [4, 12, 15].

The results for resistors is shown in Figure 4, with the red-outlined columns indicating for tests gone through these cycles with failures. The 1506 resistor was the largest package size part tested and therefore would exhibit the worst case scenario for the highest thermal stress evaluation on a passive part. Three matertial combinations survived over 2000 cycles were nickel under gold (Ni/Au) endcap finish on the polyimide substrate with $In_{80}Pb_{15}Ag_5$ solder, $Sn_{62}Pb_{36}Ag_2$ finish on the polyimide with $In_{80}Pb_{15}Ag_5$ solder, and Ni/Au finish on LTCC substrate with Ablebond 967-1 attach, all with Parylene C overcoating. It seemed that a Ni layer functioned as an adhesion layer and interdiffusion barrier and that the failure mechanism on the resistor with $Sn_{62}Pb_{36}Ag_2$ finish may be due to the absence of a Ni layer which could not structurally hold the solder.

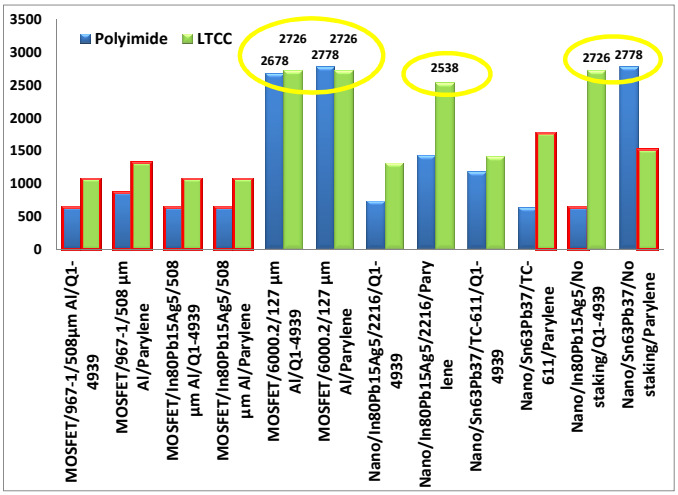

Figure 3. Summary of Experiment two for MOSFETs and nano-connectors: circled material conbinations survived over 2010 cycles without failures.

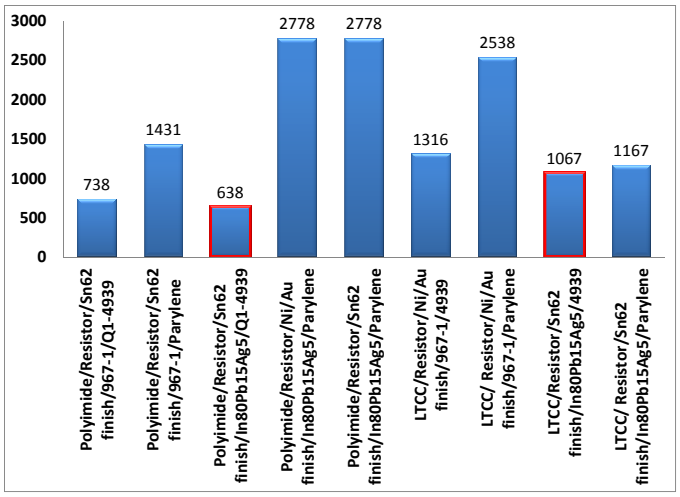

Figure 4. Summary of Experiment two for resistors.

3) Material selection for flight assembly:

Extensive testing, characterization and failure analysis were done during this technology development and evaluation phase. The flight assembly board materials combination was first recommended based on the results and analyses of the two experiments. It should be noted that the flight assembly board materials combination was finalized by not only considering the recommendations, but also the flight design and heritage.

III. TEHCNOLOGY AND SPACE QUALIFICATION

There are a number of reliability qualification standards available, but none of these existing standards addresses the reliability qualifications under the wide temperature range for space mission. A combination and integration of the stress-test-driven approach and knowledge-based approach, concentrating on the knowledge-based physics of failures methodology and application and use condition specific methodology, if applied intelligently, can be the first step. However, the most important focusing point is to be *proactive* in that the qualification activity is not treated as a simple "plan" to demonstrate a technology at the end of the development cycle, but as a "program" and a "process" which need to be integrated into the development cycle at an early stage, and re-visited and applied across every single design phase for risk mitigation and management. This requires concurrent engineering in reliability qualification for extreme environment electronics [16]. Therefore, the extensive characterization and tests, including short-term and long-term, as well as a fair amount of failure analysis, during the technology development and evaluation phase, which are described in section II, were integral part of the technology qualification process and the path to space hardware qualification.

At a more detailed level, in addition to the design-for-reliability approach during the technology and assembly board material combination development and evaluation, an application-specific assembly qualification methodology was developed and outlined, treating the assembly as a "hybrid", to qualify the assembly under the specific space radiation and wide temperature environments, i.e., 6 krad total dose over the mission life and an estimated 670 thermal cycles of -128°C to +20°C Mars environment.

The Mars environment temperature is -128°C to 20°C. Adding the estimated thermal dissipation during the mission and thermal margin during qualification, the qualification temperature for electronics was determined as -143°C to 125°C, and -120°C to 85°C for packaging and assembly board for the application-specific qualification approach.

In addition to application-specific approach, an optimized combination of component level and assembly board level qualification processes were needed to be determined for this application.

In general, there are two qualification approaches, one is more of a top-down approach which focuses on systems, and the other is a bottom-up approach which concentrates on components.

Generally, qualification at board or assembly level cannot achieve the same level of confidence compared to qualification at component level, and both system reliability analysis and component reliability analysis must be fully understood and fully implemented to ensure mission success. For some applications, a "hybrid" approach may be taken, in which board level or assembly level characterization or screening or qualification may replace component level characterization or screening or qualification to a certain degree. In those cases, the combination of component level and assembly board level qualification processes should be determined by the criticality of the assembly for the application and the level of uncertainty of both components and packaging technologies used for the assembly under the environments. In addition to cost and schedule, the key factor to consider is reliability requirement or risk acceptance for the application.

For this assembly, a high level of reliability was required and yet all the electronics and materials were not designed for the environment except for the customized op-amp. Therefore, the space qualification was focused on both component and assembly board level qualification processes on electronics and materials, minimizing the risk for technologies outside spec limits while emphasized on the reliability qualification under application target.

A. Electronics

1) Customized op-amp

Since the technology infusion was planned during the initial phase of its design and development, the technology qualification and the space qualification were integrated together for the op-amp.

The qualification baseline is MIL-PRF-38535 and MIL-PRF-38534, but with additional qualification steps to address the lower temperature operation, which includes screening and life test at low temperature [17]. A detailed qualification flow for the op-amp dice is shown in Table 3.

Table 3. Technology Qualification Flow for Op-Amp Dice

Step	Screen	Required	Reject Criteria	Sample Size
Sample Screening Requirements				
1	Wafer Level Functional Test	Test to datasheet @ room temperature only	Any part failing to meet data sheet parametric at the temperatures specified.	100%
2	Element Visual	MIL-STD-883, Method 2010, Condition A		100%
3	Serialization	Laser Serialization for traceability		100%
Qualification Requirements				
4	Sample Construction Test	DPA per MIL-STD-883, Method 5009	Any abnormal processing especially with metalization. Thinning, voids, notches, or apparent aberrations will be recorded.	5 pcs
5	Electrical	Test to datasheet @ +125C, +25C, -55C	Any part failing to meet data sheet parametric at the temperatures specified.	200 psc
6	Static Burn-in (High Temperature)	MIL-STD-883, Method 1015, 96 hours at +125C		100%
7	Electrical	Test to datasheet @ +125C, +25C, -55C	Any part failing to meet data sheet parametric at the temperatures specified.	100%
8	Dynamic Burn-in (High Temperature)	MIL-STD-883, Method 1015, 240 hours at +125C		100%
9	Electrical	Test to datasheet @ +125C, +25C, -55C	Any part failing to meet data sheet parametric at the temperatures specified.	100%
10	Life Test (Dynamic, High Temperature)	MIL-STD-883, Method 1005, 1000 hour at 125C.	Any part failing to meet data sheet parametric at the temperatures specified.	45 pcs
11	Electrical	Test to datasheet @ +125C, +25C, -55C, -143C	Any part failing to meet data sheet parametric at the temperatures specified.	45 pcs
12	Static Burn-in (Low Temperature)	MIL-STD-883, Method 1015, 96 hours at -143C		100%
13	Electrical	Test to datasheet @ +125C, +25C, -55C, -143C	Any part failing to meet data sheet parametric at the temperatures specified. Data to be reviewed for outliers	100%
14	Dynamic Burn-in (Low Temperature)	MIL-STD-883, Method 1015, 240 hours at -143C		100%
15	Electrical	Test to datasheet @ +125C, +25C, -55C, -143C	Any part failing to meet data sheet parametric at the temperatures specified. Data to be reviewed for outliers	100%
16	Life Test (Dynamic, Low Temperature)	MIL-STD-883, Method 1005, 1000-hour at -143C.	Any part failing to meet data sheet parametric at the temperatures specified. Data to be reviewed for outliers	45 pcs
17	PDA and FA			
18	Burn-in Condition Determination for Flight Parts	Qualification will determine if low temperature burn-in is needed		
Flight Parts 100% Screening Requirements				
19	Electrical	Test to datasheet @ +125C, +25C, -55C	Any part failing to meet data sheet parametric at the temperatures specified.	100%
20	Burn-in	Specifications depends on qualification results		100%
21	Electrical	Test to datasheet @ +125C, +25C, -55C	Any part failing to meet data sheet parametric at the temperatures specified.	100%
22	Part Identification			

Known good die (KGD) approach was integrated into the op-amp design and qualification because of the chip-on-board requirements. There are double bond pads on each op-amp die, shown in Figure 5. One pad is used for temporary packaging developed for burn-in purpose, and the other for the actual application wire bonding on the assembly. The bonding process was designed to ensure that the residual foot prints of the bonded wire in the pad area for burn-in or screening did not pose an issue for the assembly and assembly reliability. This was one of the key elements for the successful implementation of the op-amp qualification and application.

Radiation effects were addressed in parallel. New design on the bias circuitry was incoorporated to mitigate the analogy sensitivity as the result from the radiation evaluation during the technology evaluation. In addition, radiation evaluation as the wafer lot acceptance was performed for the flight lot. Since the annealing effect occurs at higher temperature and the operation environment was expected at be a varying operating temperature condition, radiation tests were performed at the room temperature, not at low temperature. The op-amp was predicted to perform well and meet the mission requirements.

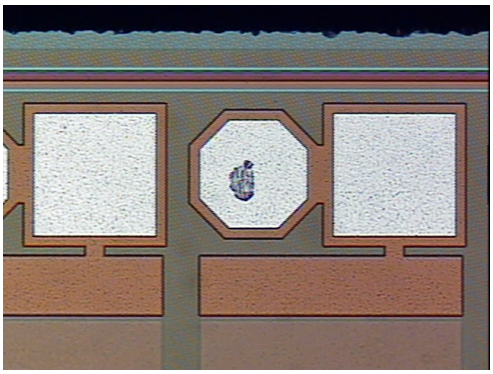

Figure 5. Double bond pads on the customized op-amp for the chip-on-board op-amp screening and qualification during technology and space qualification.

2) Large sample chatacerizatin

Figure 6 shows the outline of the space qualification flow for all electronics on the assembly. These qualification steps were determined and defined based on the technology evaluation results of each type of electronics and the baseline requirements from MIL-PRF-38534, treating the assembly as a "hybrid". In addition to the "standard steps", an element evaluation including a large sample characterization and a low temperature screening and life test were added and conducted in the technology evaluation and space qualification flow.

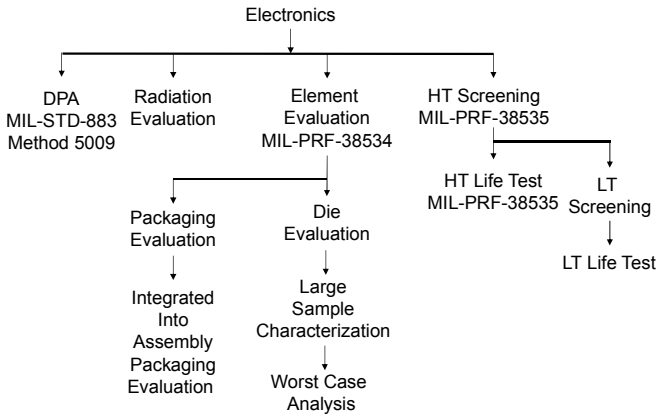

Figure 6. Outline of the space qualification flow for the electronics on the assembly.

Large Sample Characterization:

The minimum sample size for the large sample characterization including the screeening, life testing and electrical characterization on thre electronics was 22. The large sample characterization for the electrical performance was performed at temperatures of -143°C, -55°C, 25°C and 85°C, and distributions of each critical parameter for each component were derived. The information and data were used for design verification and confirmation as well as worst case analysis of the assembly across the application temperature range. The element evaluation and large sample characterization was embedded in the qualification flow in Table 3 for the op-amp.

Low Temperature Screening and Life Tests:

The low temperature screening and life tests for the electronics were to address any potential reliability issues under the lower end of the operating temperature range. Both of the tests were performed at -143°C, which was the qualification temperature decided based on the operating temperature range and margin required for qualification. The actual lowest temperature on Mars is not to be lower than 128°C. The long term reliability issue had been addressed by the design for hot carrier reliability for the op-amp, and by manufacturer's and military standard qualification for other electronics on the assembly. The screening and life tests at the low temperature were conducted to ensure there was no process induced early failures. The details of the low temperature screening and life tests are shown in Table 3 for the op-amp, and the same for the other electronics.

High Temperature and Low Temperature Screening condition for Flight Electronic Components:

The final screening process and condition for the flight electronic compoenents were based on the results of technology qualification as well as the space qualification. The screening process defined in the qualification flow were applied to the flight compoenents. It should be pointed out that, while there were some major degaration or failures of the components over the wide temperature range observed during the technology qualification, no failure occurred during the space qualification for the eletronic components selected and evaluated by the technology qualification.

B. Assesmbly Board

1) 3x of the Mission Targeted Thermal Cycle Life Time

There was no specific technology qualification step, but rather a set of technology evaluation analysis and testing for the assembly packaging materials by performing over 2000 thermal cycles on the selected material combinations during experiment one and two. The number of thermal cycling during the technology evaluation process was a close estimate to the three times (3x) of the targeted thermal cycles for the mission. However, no other flight mission requirements were added on during the technology evaluation step.

Qualification Flow:

Based on the technology evaluation results as well as the flight design and heritage, the flight assembly packaging material combinations were selected and defined. The flight assembly packaging materials went through a space qualification process not only to demonstrate a survivability of at least 3x of the mission targeted life time, in addition to meet other requirements. The outline of the space qualification flow for the assembly is shown in Figure 7.

The same as electronic technology space qualification, there was no component or packaging material failures observed during the space qualification, indicating a successful selection of the components and packaging materials on the flight assembly and a successful technology infusion into the flight application.

3x of Mission Lifetime for Qualification:

For this application, mission target thermal cycling was 670 "earth" thermal cycles of -120°C to 85°C and, therefore, the total cycles for the flight hardware were over 2010 assembly level thermal cycling with electronics and packaging materials as the three times (3x) of the targeted thermal cycles for the mission. The samples size for both technology evaluation and space qualification is 10.

Table 4 goes through the assumption and mission success probability calculation with 10 sample size using the "3x approach".

Assume one mission lifetime is L, and the failure times of the assemblies follow a normal distribution with mean of μ and standard deviation of σ. The evaluation and qualification criterion is "no failure for 10 samples during the 3x of mission lifetime", which means the event or the probability of "no failure for 10 samples during the 3x of mission lifetime" should not be a small probability event.

Apparently, the greater the difference between the mean of the failure distribution μ and mission life L is, the higher the probability of the mission success will be.

If 3x of the mission lifetime $3L$ is at the point of $\mu-\sigma$, i.e. $\mu-\sigma = 3L$, then the probability of one sample not to fail for 3x of mission lifetime (column B in Table 4) is $Pr(x>3L) = Pr(x>(\mu-\sigma)) = 0.841344746$, and hence the probability of 10 samples without failure for 3x of mission lifetime (column C in Table 4) will be $0.841344746^{10} = 0.177721459$, which is a small probability event. If we consider a small probability event is an event with a probability of less than 0.5, then the 3x of mission lifetime needs to be the same as or shorter than $(\mu-1.5*\sigma)$, where the probability of 10 samples without failure for 3x of mission lifetime is larger than 0.5.

Column D in Table 4 gives the probability of one flight assembly not to fail during one mission lifetime given that 10 samples without failure for 3x of mission lifetime.

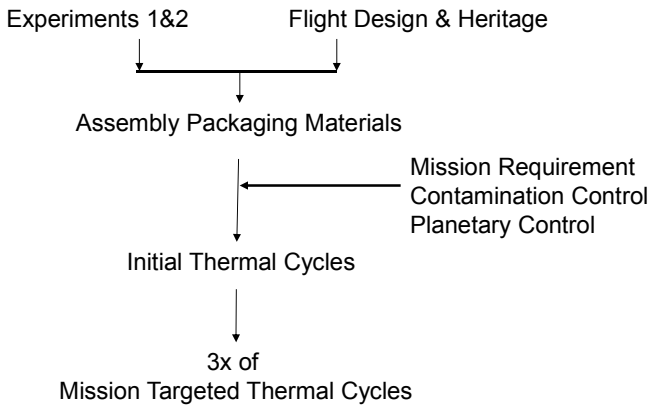

Figure 7. Outline of the space qualification flow for the assembly.

Table 4. Assumption and Mission Success Probability using 3x Approach

Assume μ - y*σ = 3L			
(A) y	(B) Probability of one sample not to fail for 3 times of mission lifetime Pr (x > 3L) = Pr (x > (μ-y*σ))	(C) Probability of 10 samples w/o failure for 3 times of mission lifetime Pr (x > 3L) ^ 10	(D) Probability of one flight assembly not to fail during one mission lifetime given that 10 samples w/o failure for 3 times of mission lifetime Pr (x > L)
1	0.841344746	0.177721459	0.998650102
1.5	0.933192799	0.500857046	0.999767371
2	0.977249868	0.794431040	0.999968329
2.5	0.993790335	0.939610121	0.999996602
3	0.998650102	0.986582725	0.999999713

2) Planetary Protection

It should be noted that, in addition to the 3x mission life thermal cycle requirement, there were other requirements by the specific flight mission, the contamination control and planetary control planetary protection. Those requirements, such as planetary test by dry heat microbial reduction techniques aiming to prevent biological contamination, was a required step and was included in the assembly space qualification.

C. Component versus Assembly

Generally, qualification at board or assembly level cannot achieve the same level of confidence compared to qualification at component level [18], since not all the targeted operating conditions of the components can be individually tested at the assembly level or at the elevated temperature only achievable at the component level.

In addition, it has been demonstrated that even with the *same* Mean Time to Failure (MTTF), components operating in the decreasing failure rate region or infant mortality region yield lower level of the system reliability compared to the components operating in the constant failure rate region [19]. Therefore, all the components went through the upscreening process at the component level to ensure that no early component failures.

As a high level of reliability was required for this assembly, the space qualification was focused on both component and assembly board level qualification processes, no component level qualification replaced by assembly level.

IV. SUMMARY

This paper describes the details for the qualification of a motor drive electronics assembly for Mars Curiosity Rover under space extreme environments. Both component and assembly board level qualification were performed as a high level reliability was required and the uncertainty of the technologies under extreme space environments was addressed.

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