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Use of a Frequency Divider to Evaluate an SOI NAND Gate Device, Type CHT-7400, for Wide Temperature Applications

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Scope

Frequency dividers constitute essential elements in designing phase-locked loop circuits and microwave systems. In addition, they are used in providing required clocking signals to microprocessors and can be utilized as digital counters. In some applications, particularly space missions, electronics are often exposed to extreme temperature conditions. Therefore, it is required that circuits designed for such applications incorporate electronic parts and devices that can tolerate and operate efficiently in harsh temperature environments. While present electronic circuits employ COTS (commercial-off-the-shelf) parts that necessitate and are supported with some form of thermal control systems to maintain adequate temperature for proper operation, it is highly desirable and beneficial if the thermal conditioning elements are eliminated. Amongst these benefits are: simpler system design, reduced weight and size, improved reliability, simpler maintenance, and reduced cost. Devices based on silicon-on-insulator (SOI) technology, which utilizes the addition of an insulation layer in the device structure to reduce leakage currents and to minimize parasitic junctions, are well suited for high temperatures due to reduced internal heating as compared to the conventional silicon devices, and less power consumption. In addition, SOI electronic integrated circuits display good tolerance to radiation by virtue of introducing barriers or lengthening the path for penetrating particles and/or providing a region for trapping incident ionization. The benefits of these parts make them suitable for use in deep space and planetary exploration missions where extreme temperatures and radiation are encountered. Although designed for high temperatures, very little data exist on the operation of SOI devices and circuits at cryogenic temperatures. In this work, the performance of a divide-by-two frequency divider circuit built using COTS SOI logic gates was evaluated over a wide temperature range and thermal cycling to determine suitability for use in space exploration missions and terrestrial fields under extreme temperature conditions.

Test Procedure

The divide-by-two frequency divider circuit was built using COTS SOI NAND logic gates that were introduced recently by CISSOID Corporation. Three of these quad 2-input CHT-7400 NAND gates were used and were connected in a D-type flip-flop, master-slave configuration. Frequency division is achieved by feeding the input pulse train into the clock input, and connecting the negated output (Q-bar) to the D input, as shown in Figure 1. The circuit utilized high temperature polyimide board, NP0 ceramic capacitors, Teflon-insulated wires, and high temperature (300 °C) solder. A photograph of the circuit board is shown in Figure 2, and the manufacturer's specifications for the CHT-7400 NAND gate are shown in Table I [1].

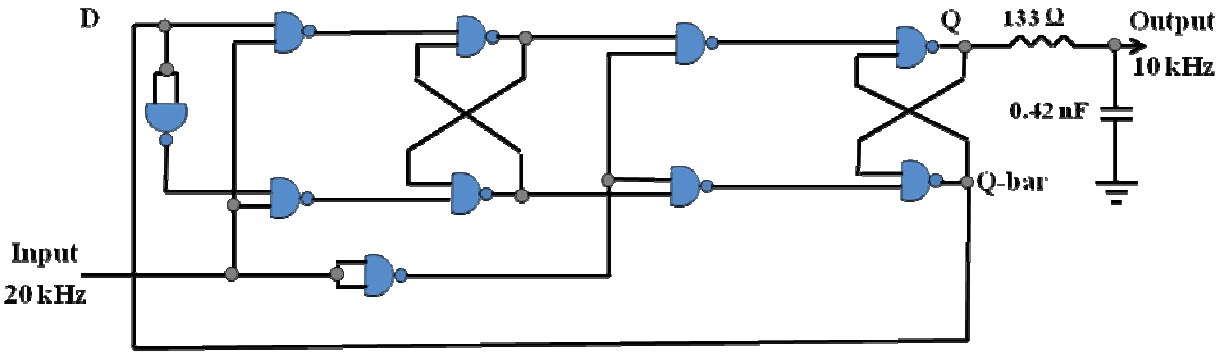


Figure 1. Schematic of the divide-by-two frequency divider circuit.

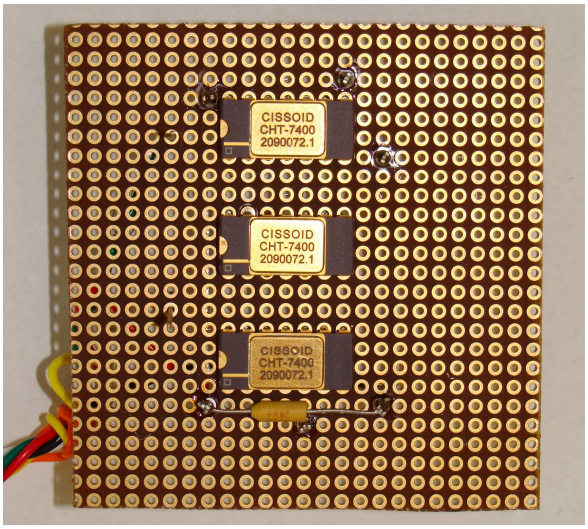


Figure 2. Frequency divider test circuit board.

Table I. Specifications of CISSOID CHT-7400 NAND Gate [1].

Parameter	**Symbol**	**CHT-7400**
Voltage Supply (V)	V_{DD}	3.3 to 5
Quiescent Current @ 225 °C (µA)	I_{DD}	7.1
Operating Temperature (°C)	T_{oper}	-55 to +225
Rise Time (ns)	t_r	7.4
Fall Time (ns)	t_f	7.8
Propagation Delay Time (ns)	τ_{PLH}	15.3
Propagation Delay Time (ns)	τ_{PHL}	16.6
Package		DIL-14
Lot Number		2090072.1

Operation of the SOI-based frequency divider circuit was investigated as a function of temperature between -192 °C and +225 °C. An Agilent Function Generator, Model 33120A, was used to provide a 20 kHz square-wave clock signal as the input. Performance characterization of the divider was obtained in terms of output frequency, rise and fall times of the output signal, signal delay time, output duty cycle, and circuit supply current at specific test temperatures. The delay time, t_{PHL}, is defined as the delay experienced by the output to follow the change in the input from going low to high state, taken at the 50% level of both signals. The test temperature points were -192, -175, -150, -100, -50, 0, +25, +50, +100, +150, +175, +200, and +225 °C. A LeCroy LT374 Digital Scope was used to measure the transition times and to capture the output waveforms. A temperature rate of change of 10 °C per minute was used, and a soak time of at least 20 minutes was allowed at every test temperature. Restart capability at extreme temperatures, i.e. power switched on while the circuit was soaking at the test temperature of either -192 or +225 °C, was also investigated. In addition, the effects of thermal cycling under a wide temperature range on the operation of this divider circuit were determined. The device was exposed to a total of 12 cycles between -192 °C and +225 °C at a temperature rate of 10 °C/minute. Following the thermal cycling, measurements were then performed at the test temperatures of -192, +25, and +225 °C.

Test Results

Temperature Effects

Waveforms of the clock input signal and the resulting output signal of the frequency divider recorded at room temperature are shown in Figure 3. These waveforms were also obtained, as mentioned earlier, at the test temperatures of -192, -175, -150, -100, -50, 0, +25, +50, +100, +150, +175, +200, and +225 °C. No major change was observed in the shape or magnitude of these waveforms as test temperature was changed throughout the range of -192 °C to +225 °C. For illustrative purposes, therefore, only those waveforms obtained at the extreme temperature, i.e. -192 °C and +225 °C, are also presented here as shown in Figures 4 and 5, respectively.

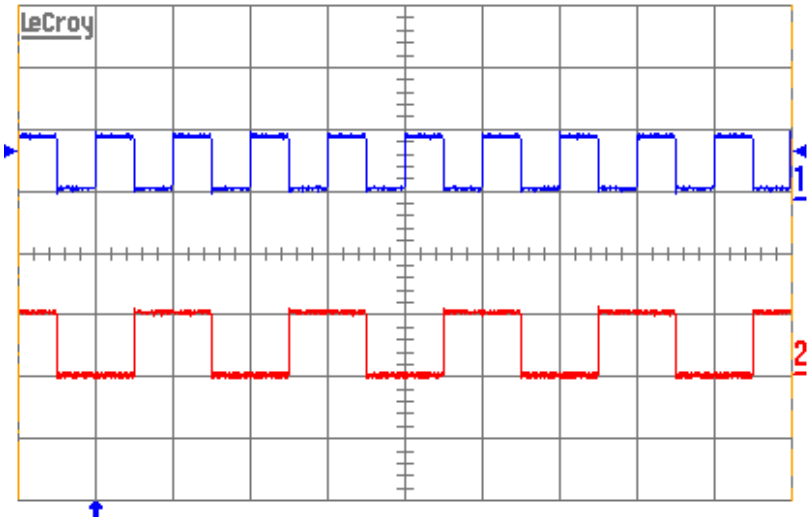


Figure 3. Input (trace 1) and output (trace 2) signals at +25°C.
(Scale: Vertical 5 V/div; Horizontal 50 µs/div)

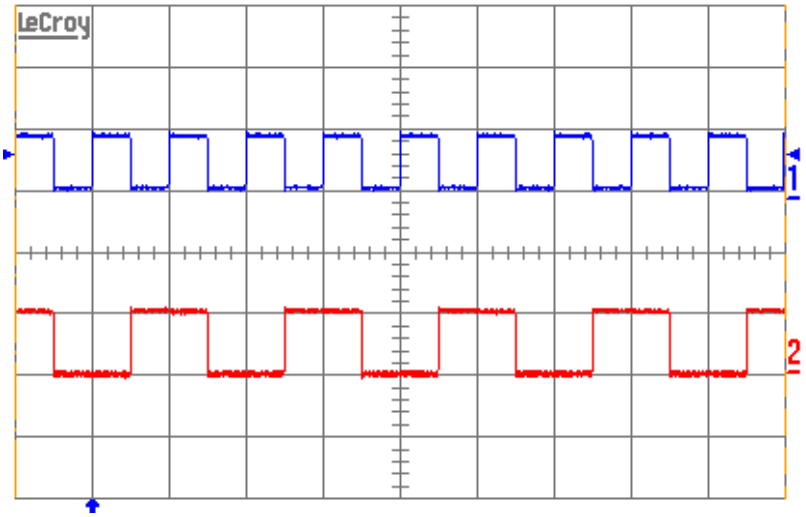


Figure 4. Input (trace 1) and output (trace 2) signals at -192°C.
(Scale: Vertical 5 V/div; Horizontal 50 µs/div)

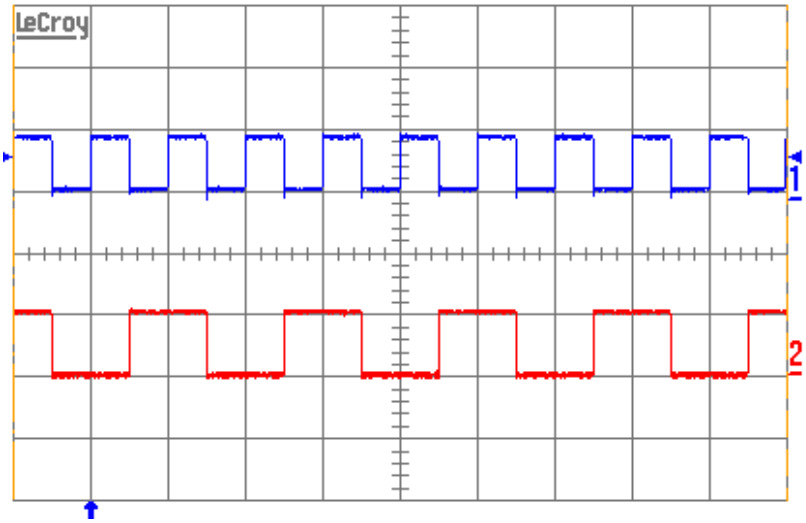


Figure 5. Input (trace 1) and output (trace 2) signals at +225°C.
(Scale: Vertical 5 V/div; Horizontal 50 µs/div)

Figure 6 depicts the variation in the rise and fall times of the output signal as a function of temperature. In general, the rise times showed a slight but continuous increase in value as temperature was increased throughout the test temperature range from -192 °C to +225 °C. Similar trend was observed for the effect of temperature on the fall time except its increase was slightly higher in the high temperature region between +100 °C and +225 °C. The delay time between the output and the input signals is shown in Figure 7 as a function of temperature. It can be seen that this property did not display any dependency on temperature as it maintained a steady value of about 25 ns throughout the test temperature regime. Similarly, the duty cycle of the output signal remained steady at 50% irrespective of the test temperature, as shown in Figure 8.

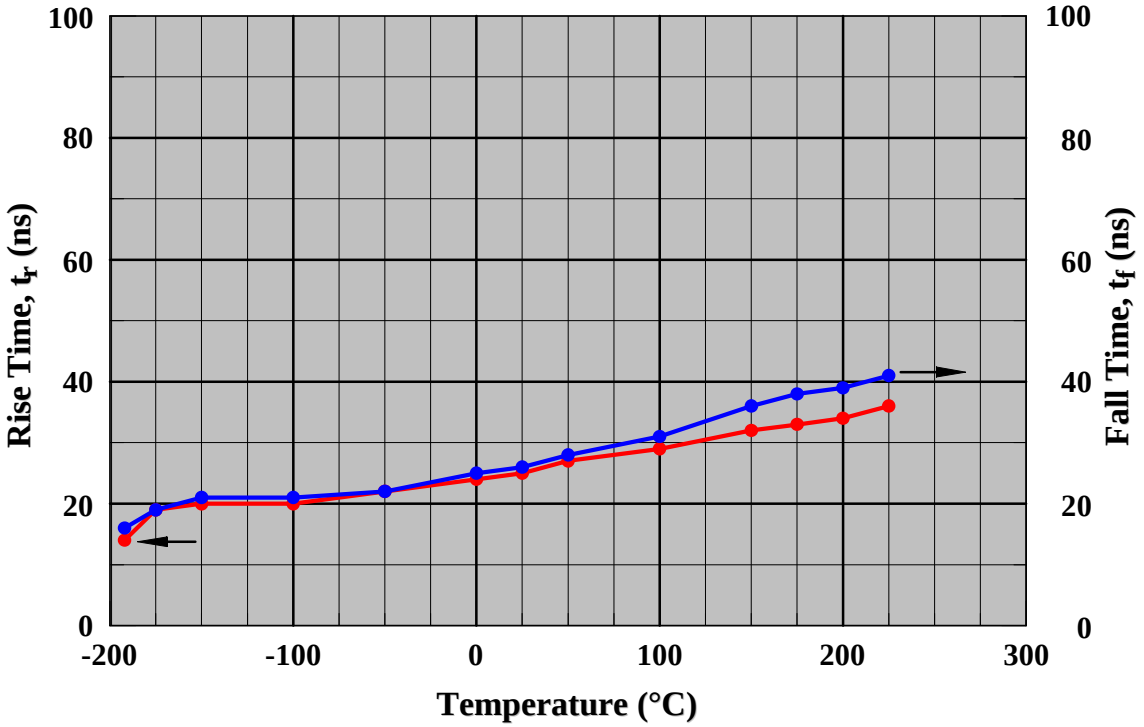


Figure 6. Rise and fall times of the output signal as a function of temperature.

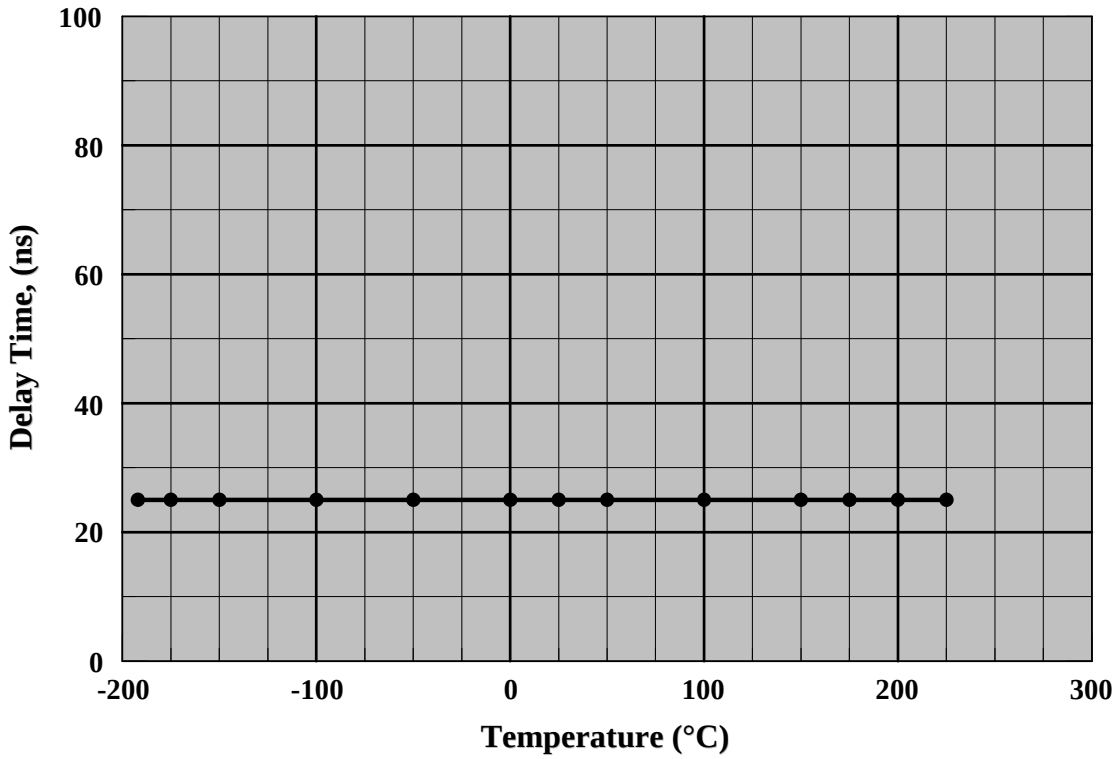


Figure 7. Transition delay times from input to output signal as a function of temperature.

The input current of the frequency divider circuit exhibited an inverse relationship with temperature as shown in Figure 9. It can be seen that the current decreased, in almost a linear fashion, as the test temperature was increased from -192 °C to +225 °C. This decrease in current, which amounted from a magnitude of 2.53 mA at -192 °C to about 1.80 mA at +225°C, is beneficial particularly at high temperatures where internal heating as well as operational temperatures tend to degrade the behavior of most electronic parts.

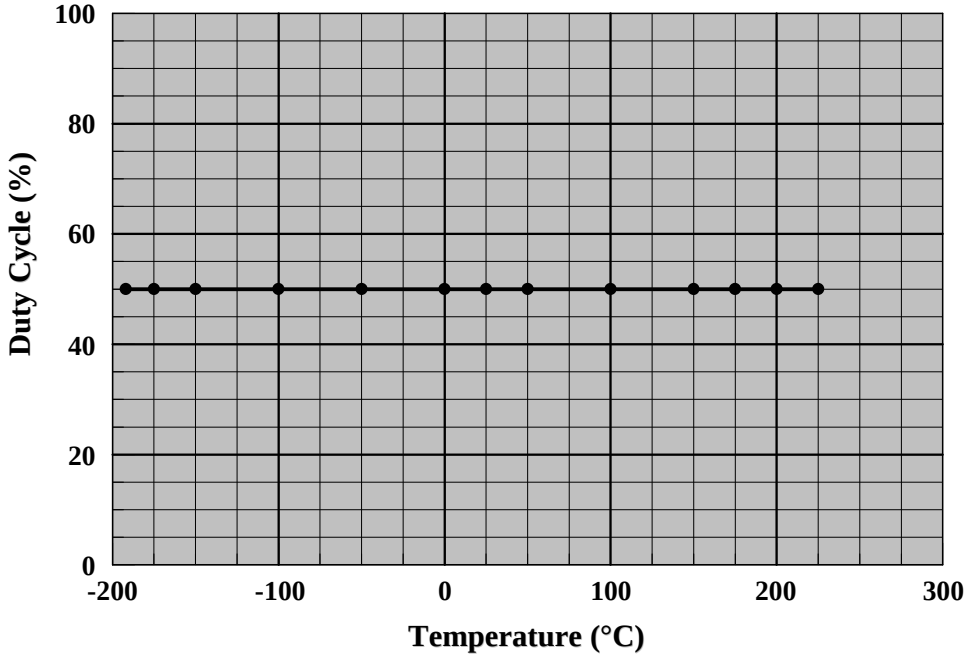


Figure 8. Duty cycle of the output signal versus temperature.

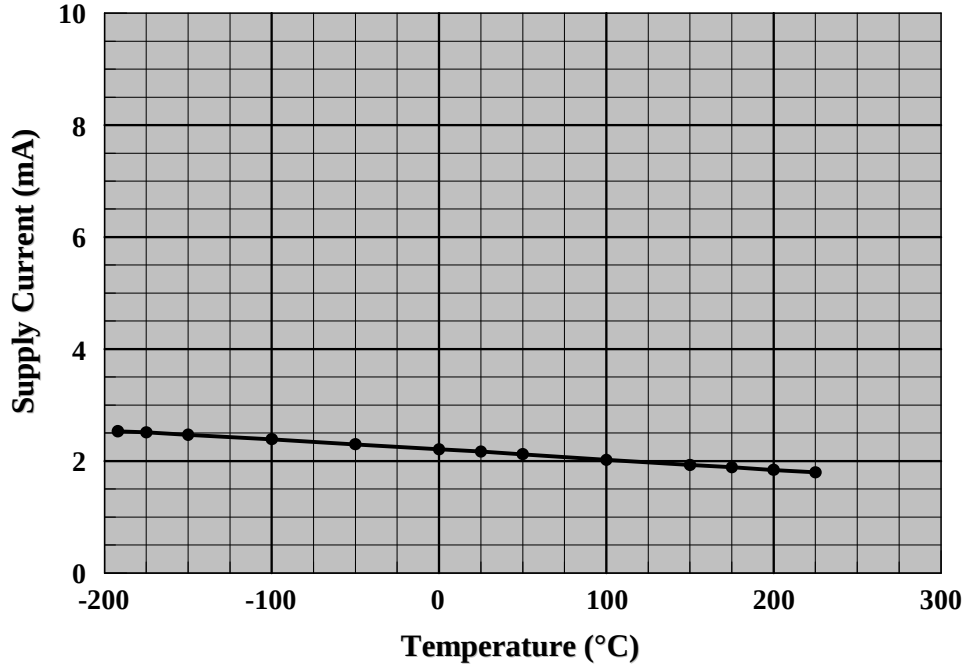


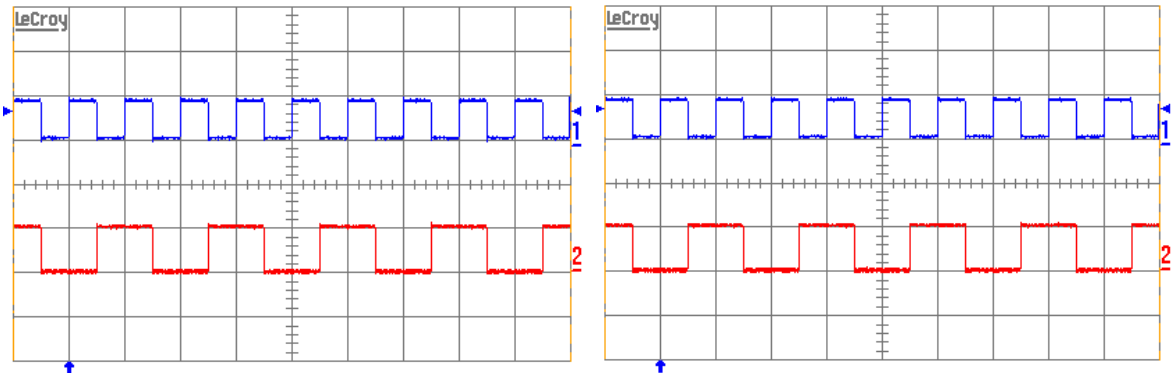
Figure 9. Supply current of the frequency divider circuit as a function of temperature.

Restart at Extreme Temperatures

Restart capability of the frequency divider circuit at extreme temperatures was also investigated by allowing it to soak for at least 20 minutes at each of the test temperatures of -192 °C and +225 °C without electrical bias. Power was then applied to the divider circuit, and measurements were taken on the output characteristics. The circuit was able to successfully restart at both extreme temperatures and the results obtained were the same as those attained earlier for both temperatures.

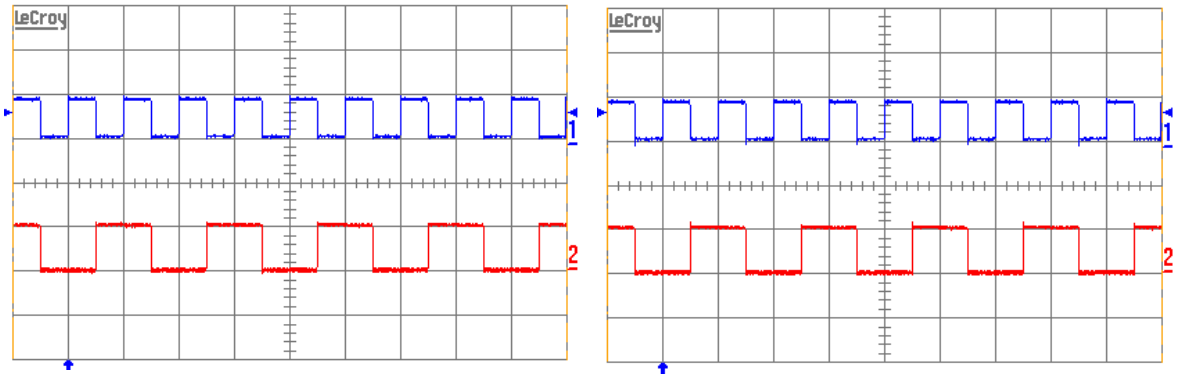
Effects of Thermal Cycling

The effects of thermal cycling under a wide temperature range on the operation of the frequency divider were investigated by subjecting it to a total of 12 cycles between -192 °C and +225 °C at a temperature rate of 10 °C/minute. A dwell time of 20 minutes was applied at the extreme temperatures. Measurements of the investigated parameters were then taken as a function of temperature. A comparison of the waveforms of the clock input and the output signals at the selected test temperatures of +25, -192, and +225 °C for pre- and post-cycling conditions are shown in Figures 10, 11, and 12, respectively. It can be clearly seen that the post-cycling output signals at any given test temperature were the same as those obtained prior to cycling. Similarly, no significant changes were registered between the pre- and post-cycling values of the output's rise and fall times, signal transition delay time, output duty cycle, and the circuit's supply current, as depicted in Table II at the selected three test temperatures. Therefore, it can be concluded that the extreme temperature exposure and the thermal cycling did not induce much change in the behavior of this frequency divider circuit. This limited thermal cycling also appeared to have no effect on the structural integrity of the SOI NAND gates device as no structural deterioration or packaging damage was observed.



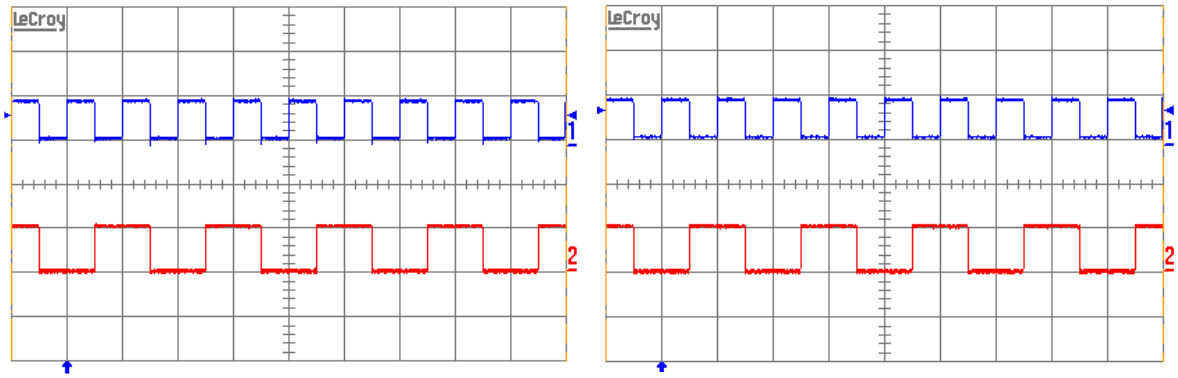
Pre-cycling Post-cycling

Figure 10. Pre- & post-cycling signals of input (trace 1) and output (trace 2) at +25°C.



Pre-cycling Post-cycling

Figure 11. Pre- & post-cycling signals of input (trace 1) and output (trace 2) at -192°C.



Pre-cycling Post-cycling

Figure 12. Pre- & post-cycling signals of input (trace 1) and output (trace 2) at +225°C.

Table II. Pre- & post-cycling values of rise, fall, & delay times, duty cycle, and supply current.

	Rise Time t_r (ns)		**Fall Time t_f (ns)**		**Delay Time (ns)**		**Duty Cycle (%)**		**Supply Current (mA)**	
Temp. (°C)	Prior	Post	Prior	Post	Prior	Post	Prior	Post	Prior	Post
+25	25	26	26	26	25	25	50	50	2.17	2.16
-192	14	19	16	20	25	25	50	50	2.53	2.53
+225	36	35	41	40	25	25	50	50	1.80	1.81

Conclusions

A CISSOID SOI Quad 2-Input NAND device, type CHT-7400, was evaluated for wide temperature range operation between -192 °C and +225 °C. In the evaluation, three of the devices were connected into a divide-by-two frequency divider configuration. At various temperatures, the output gate was characterized in terms of its output frequency, rise and fall times, and output duty cycle; and the circuit supply current was also measured. The effects of thermal cycling under a wide temperature range on its operation and stability, as well as restart capability at extreme temperatures was also investigated. The output gate and the frequency divider were able to exhibit and maintain good operation between -192 °C and +225 °C without undergoing any major changes in characteristics. The output frequency of the circuit was always exactly half of the input frequency. The limited thermal cycling performed on the circuit also had no effect on its performance, and the divider was able to successfully restart at each of the extreme temperatures of -192 °C and +225 °C. The ceramic packaging of the SOI NAND devices was also not affected by the extreme temperature exposure. These preliminary results indicate that the CHT-7400 SOI NAND device and the SOI-based frequency divider could potentially be used under wide temperature range. Further testing and long-term cycling, however, need to be performed on the device and circuit in order to establish their suitability and reliability for extended use in space exploration missions under extreme temperature environments.

References

[1]. CISSOID Corporation "CHT-7400 High Temperature, Quad 2-Input NAND Gate" Data Sheet, Doc. DS-080204, V01.02, January 23, 2009. http://www.CISSOID.com

Acknowledgements

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