

Enabling large focal plane arrays through mosaic hybridization

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ABSTRACT

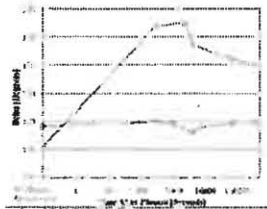
We have demonstrated advances in mosaic hybridization that will enable very large format far-infrared detectors. Specifically we have produced electrical detector models via mosaic hybridization yielding superconducting circuit paths by hybridizing separately fabricated sub-units onto a single detector unit. The detector model was made on a 100mm diameter wafer while four model readout quadrant chips were made from a separate 100mm wafer. The individually fabricated parts were hybridized using a flip-chip bonder to assemble the detector-readout stack. Once all of the hybridized readouts were in place, a single, large and thick silicon substrate was placed on the stack and attached with permanent epoxy to provide strength and a Coefficient of Thermal Expansion match to the silicon components underneath. Wirebond pads on the readout chips connect circuits to warm readout electronics; and were used to validate the successful superconducting electrical interconnection of the model mosaic-hybrid detector. This demonstration is directly scalable to 150 mm diameter wafers, enabling pixel areas over ten times the area currently available. → 40,000 PIXEL ARRAYS

MOTIVATION

- Next generation of large-scale science experiments studying the universe will require large format, background limited, detector arrays containing tens of thousands of pixels¹.
- Currently, no existing detector for λ longer than 40 μm that can meet the stated science goals.
- A large community of scientists submitted clear recommendations towards the New Worlds, New Horizons decadal survey in astronomy and astrophysics, including the need for novel detector array technologies with an order of magnitude or more increase in the format available today²

PLASMA CLEANING

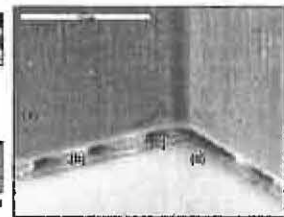
- Indium oxidizes readily in air
- Hybrid is created in air, indium cold welds to detector
- In_2O_3 has poor adhesion, presents electrical barriers
- Plasma reduces the oxide and replaces it with indium-nitride, ruptures more easily than In_2O_3
- Used ellipsometry to track surface film of the indium



Ellipsometry measurements of control (C) and plasma cleaned (O) samples. The control sample stays high, indicating native oxide. The plasma-cleaned sample jumps and plateaus high due to surface formed indium-nitride passivation.

INDIUM HYBRIDIZATION

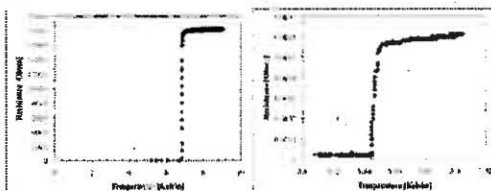
- Over 200,000 indium bumps
- 0.4 g-force/bump
- Alignment tolerance $\pm 2\mu\text{m}$
- Laser Levelling, $\pm 1\mu\text{m}$ parallelism
- Pull-Tested to 100 lbs. of force
- Post hybridization anneal for 16 Hrs. at 120°C enhances the cold weld joint.
- Final gap measurement all quads, 4.1 $\mu\text{m} \pm 1.0\mu\text{m} \rightarrow$ compression of 5.4 μm .



Shown above is an SEM image of a detector corner after hybridization. (a) Detector Wall, (b) Indium, (c) Under-Bump-Metal, (d) Substrate

SUPERCONDUCTING CIRCUITRY

- Tested using pumped He dewar
- 4-wire measurements, Labview DAQ
- Successfully made a superconducting cold-weld joint
- Measurement range of 2G and an excitation of 2mV $\rightarrow$ critical current > 1mA
- Successful pixel rate of 91% of testable channels



Left: A plot of R vs. T for our molybdenum nitride film. The resistance below the To is not zero at this point, as the indium has not yet gone through its transition. Right: A plot of R vs. T for our indium. The overall circuit is superconducting at this point as the resistance is pegged low.

CURRENT DETECTOR ARCHITECTURE

- The backshort-under-grid (BUG) architecture
- Currently in use with two instruments
- GISMO^{3,4}
 - Utilizes background limited TES bolometers
 - BUG, reflective backshort
 - 6x16 array of 2mm pitch, 50 μm walls between pixels
 - 2D wiring to linear SQUID MUX readout
 - FACILITY INSTRUMENT AT IRAM 30m TELESCOPE
- PIPER⁵ (currently in development)
 - Utilizes background limited TES bolometers
 - BUG, reflective backshort
 - 32x40 array of 1mm pitch, 50 μm walls
 - 3D wiring to 2D SQUID MUX readout



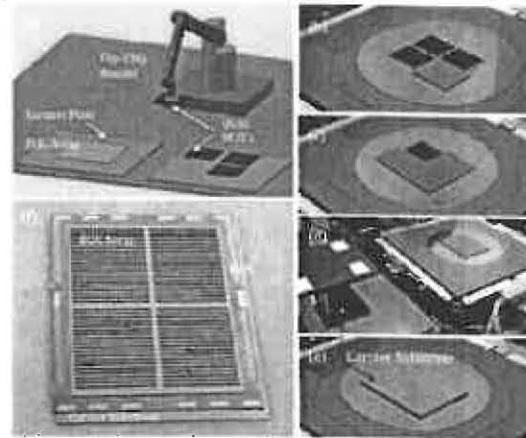
PIPER shown as right in test package using linear-MUX's

Beyond PIPER

- Many thousands of pixels requires a technology to scale up the focal plane.
- Straight scaling detector and MUX $\rightarrow$ significant increase in cost and development.
- Mosaic tiling the existing MUX architecture could yield a more elegant and cost effective approach, producing space-worthy, far-infrared to sub-mm, highly sensitivity bolometer arrays on a scale never before demonstrated.

MOSAIC HYBRIDIZED MODELS

The sequence below illustrates the mosaic build process. (a) is a sketch of the assembly process, showing the flip-chip bonder placing mosaic quadrants of readout chips onto a single BUG array. Images (b) - (f) are photographs taken of parts during the assembly process, starting with the population of the BUG array with readout quadrants (b) - (d). Next (e), final placement of a carrier substrate on the readout quadrants for support. (f), the finished array from the front-side, highlights each component; the carrier, the readout quads and the singular detector grid on top.



SUMMARY

- Demonstrated mosaic hybridization process
- Superconducting indium joints in all quadrants, 91% yield
- Scalable to 150mm wafers
- Technology demonstration toward background limited arrays of 40,000 pixels

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