twinax connector attachment points. The differential impedance is inversely proportional to the square root of the relative dielectric constant. This increases the differential impedance and thus reduces the above described impedance discontinuity. The differential via hole impedance can also be increased in the same manner. This technique can be extended to multiple smaller drilled holes as well as tapered holes (i.e., big in the middle followed by smaller ones diagonally).

This work was done by Sal Navidi, Rodell Agdinaoay, and Keith Walter of Honeywell Aerospace for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809.

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)}, to Honeywell Aerospace. Inquiries concerning licenses for its commercial development should be addressed to:

Honeywell Aerospace
P.O. Box 52199
Phoenix, AZ 85072

Refer to MSC-24855-l, volume and number of this NASA Tech Briefs *issue, and the page number.*

SpaceCube Version 1.5

This processing system is suited for any sub-orbital application that requires a compact solution with high-data-rate storage capability and high-performance processing.

Goddard Space Flight Center, Greenbelt, Maryland

SpaceCube 1.5 is a high-performance and low-power system in a compact form factor. It is a hybrid processing system consisting of CPU (central processing unit), FPGA (field-programmable gate array), and DSP (digital signal processor) processing elements. The primary processing engine is the Virtex-5 FX100T FPGA, which has two embedded processors. The SpaceCube 1.5 System was a bridge to the SpaceCube 2.0 and SpaceCube 2.0 Mini processing systems. The SpaceCube 1.5 system was the primary avionics in the successful SMART (Small Rocket/Spacecraft Technology) Sounding Rocket mission that was launched in the summer of 2011.

For SMART and similar missions, an avionics processor is required that is reconfigurable, has high processing capability, has multi-gigabit interfaces, is low power, and comes in a rugged/compact form factor. The original SpaceCube 1.0 met a number of the criteria, but did not possess the multi-gigabit interfaces that were required and is a higher-cost system. The SpaceCube 1.5 was designed with those mission requirements in mind.

The SpaceCube 1.5 features one Xilinx Virtex-5 FX100T FPGA and has excellent size, weight, and power characteristics [4×4×3 in. (≈10×10×8 cm), 3 lb (≈1.4 kg), and 5 to 15 W depending on the application]. The estimated computing power of the two PowerPC 440s in the Virtex-5 FPGA is 1100 DMIPS each. The SpaceCube 1.5 includes two Gigabit Ethernet (1 Gbps) interfaces as well as two SATA-I/II interfaces (1.5 to 3.0 Gbps) for recording to data drives. The SpaceCube 1.5 also features DDR2 SDRAM (double data rate synchronous dynamic random access memory); 4-Gbit Flash for storing application code for the CPU, FPGA, and DSP processing elements; and a Xilinx Platform Flash XL to store FPGA configuration files or application code.

The system also incorporates a 12 bit analog to digital converter with the ability to read 32 discrete analog sensor inputs. The SpaceCube 1.5 design also has a built-in accelerometer. In addition, the system has 12 receive and transmit RS-422 interfaces for legacy support. The SpaceCube 1.5 processor card represents the first NASA Goddard design in a compact form factor featuring the Xilinx Virtex-5. The SpaceCube 1.5 incorporates backward compatibility with the SpaceCube 1.0 form factor and stackable architecture. It also makes use of low-cost commercial parts, but is designed for operation in harsh environments.

This work was done by Alessandro Geist, Michael Lin, Tom Flatley, and David Petrick of Goddard Space Flight Center. Further information is contained in a TSP (see page 1).
GSC-15936-1