# Electronics/Computers

## Ultra-Wideband, Dual-Polarized, Beam-Steering P-Band Array Antenna

**The novel design geometry can be scaled with minor modifications.**

*Goddard Space Flight Center, Greenbelt, Maryland*

A dual-polarized, wide-bandwidth (200 MHz for one polarization, 100 MHz for the orthogonal polarization) antenna array at P-band was designed to be driven by NASA's EcoSAR digital beam former. EcoSAR requires two wide P-band antenna arrays mounted on the wings of an aircraft, each capable of steering its main beam up to 35° off-boresight, allowing the twin radar beams to be steered at angles to the flight path. The science requirements are mainly for dual-polarization capability and a wide bandwidth of operation of up to 200 MHz if possible, but at least 100 MHz with high polarization port isolation and low cross-polarization. The novel design geometry can be scaled with minor modifications up to about four times higher or down to about half the current design frequencies for any application requiring a dual-polarized, wide-bandwidth steerable antenna array.

EcoSAR is an airborne interferometric P-band synthetic aperture radar (SAR) research application for studying two- and three-dimensional fine-scale measurements of terrestrial ecosystem structure and biomass, which will ultimately aid in the broader study of the carbon cycle and climate change. The two 2×8 element P-band antenna arrays required by the system will be separated by a baseline of about 25 m, allowing for interferometry measurements. The wide 100-to-200-MHz bandwidth dual-polarized beams employed will allow the determination of the amount of biomass and even tree height on the ground.

To reduce the size of the patches along the boresight dimension in order to fit them into the available space, two techniques were employed. One technique is to add slots along the edges of each patch where the main electric currents are expected to flow, and the other technique is to bend the central part of the patch away from the ground plane. The latter also facilitates higher mechanical rigidity.

The high port isolation of more than 40 dB was achieved by employing a highly symmetrical feed mechanism for each pair of elements: three apertures coupling to the patch elements were placed along the two symmetry lines of the antenna element pair. Two apertures were used in tandem to excite two of the stacked patch elements for one polarization; the other was used to excite one element from one side and the other element from the other side, opposite in phase, taking care of the remaining polarization. The apertures narrow down to a small gap where they are excited by a crossing microstrip line to prevent any asymmetrical excitation of the two sides of the aperture gap, minimizing port-to-port coupling.

Using patches that are non-planar leads to higher mechanical rigidity and smaller patch sizes to fit into the available space. Aperture coupling minimizes direct metal-to-metal connections. Using an aperture coupling feed mechanism results in a feed network for two antenna elements with a total of three feed points, plus one simple in-phase combiner to reduce it to two ports. It greatly reduces the complexity of the alternative, but more conventional, way of feeding a pair of two dual-polarized elements with high port isolation.

*This work was done by Cornelis du Toit of DSFG for Goddard Space Flight Center. Further information is contained in a TSP (see page 1).* GSC-16778-1

## Centering a DDR Strobe in the Middle of a Data Packet

*Lyndon B. Johnson Space Center, Houston, Texas*

The Orion CEV Northstar ASIC (application-specific integrated circuit) project required a DDR (double data rate) memory bus driver/receiver (DDR PHY block) to interface with external DDR memory. The DDR interface (JESD79C) is based on a source synchronous strobe (DQS\) that is sent along with each packet of data (DQ). New data is provided concurrently with each edge of strobe and is sent irregularly. In order to capture this data, the strobe needs to be delayed and used to latch the data into a register.

A circuit solves the need for training a DDR PRY block by incorporating a PVT-compensated delay element in the strobe path. This circuit takes an external reference clock signal and uses the regular clock to calibrate a known delay through a data path. The compensated delay DQS signal is then used to capture the DQ data in a normal register. This register structure can be configured as a FIFO (first in first out), in order to transfer data from the DDR domain to the system clock domain. This design is different in that it does not rely upon the need for training the system response, nor does it use a PLL (phase locked loop) or a DLL (delay locked loop) to provide an offset of the strobe signal.

The circuit is created using standard ASIC building blocks, plus the PVT (process, voltage, and temperature) compensated delay line. The design uses a globally available system clock as a reference, alleviating the need to operate synchronously with the remote memory. The reference clock conditions the PVT compensated delay line to provide a predetermined amount of delay to any data signal that passes through this delay line. The delay line is programmed in degrees of offset, so that one could think of the clock period representing 360° of delay. In an ideal environment, delaying the strobe 1/4 of a clock cycle (90°) would place the strobe in the middle of the data packet. This delayed strobe can then be used to clock the data into a register, satisfying setup and hold requirements of the system.

*This work was done by Michael Johnson, Dave Nelson, James Seefeldt, Weston Roper, and Craig Passow of Honeywell for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809.*

*Title to this invention has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457(f)}, to Honeywell. Inquiries concerning licenses for its commercial development should be addressed to:*

*Honeywell*
*P.O. Box 52199*
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*Refer to MSC-24931-1, volume and number of this* NASA Tech Briefs *issue, and the page number.*

# Using a Commercial Ethernet PHY Device in a Radiation Environment

*Lyndon B. Johnson Space Center, Houston, Texas*

This work involved placing a commercial Ethernet PHY on its own power boundary, with limited current supply, and providing detection methods to determine when the device is not operating and when it needs either a reset or power-cycle. The device must be radiation-tested and free of destructive latch-up errors.

The commercial Ethernet PHY's own power boundary must be supplied by a current-limited power regulator that must have an enable (for power cycling), and its maximum power output must not exceed the PHY's input requirements, thus preventing damage to the device. A regulator with configurable output limits and short-circuit protection (such as the RHFL4913, rad hard positive voltage regulator family) is ideal. This will prevent a catastrophic failure due to radiation (such as a short between the commercial device's power and ground) from taking down the board's main power.

Logic provided on the board will detect errors in the PHY. An FPGA (field-programmable gate array) with embedded Ethernet MAC (Media Access Control) will work well. The error detection includes monitoring the PHY's interrupt line, and the status of the Ethernet's switched power. When the PHY is determined to be non-functional, the logic device resets the PHY, which will often clear radiation induced errors. If this doesn't work, the logic device power-cycles the FPGA by toggling the regulator's enable input. This should clear almost all radiation induced errors provided the device is not latched up.

*This work was done by Jeremy Parks, Michael Arani, and Roberto Arroyo of Honeywell Aerospace for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809.*

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# Submerged AUV Charging Station

## Potential uses include studying ocean climate change, pollution, salinity, and currents.

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Autonomous Underwater Vehicles (AUVs) are becoming increasingly important for military surveillance and mine detection. Most AUVs are battery powered and have limited lifetimes of a few days to a few weeks. This greatly limits the distance that AUVs can travel underwater. Using a series of submerged AUV charging stations, AUVs could travel a limited distance to the next charging station, recharge its batteries, and continue to the next charging station, thus traveling great distances in a relatively short time, similar to the Old West "Pony Express."

One solution is to use temperature differences at various depths in the ocean to produce electricity, which is then stored in a submerged battery. It is preferred to have the upper buoy submerged a reasonable distance below the surface, so as not to be seen from above and not to be inadvertently destroyed by storms or ocean going vessels. In a previous invention, a phase change material (PCM) is melted (expanded) at warm temperatures, for example, 15 °C, and frozen (contracted) at cooler temperatures, for example, 8 °C.

Tubes containing the PCM, which could be paraffin such as pentadecane, would be inserted into a container filled with hydraulic oil. When the PCM is melted (expanded), it pushes the oil out into a container that is pressurized to about 3,000 psi (≈20.7 MPa). When a valve is opened, the high-pressure oil passes through a hydraulic motor, which turns a generator and charges a battery. The low-pressure oil is finally reabsorbed into the PCM canister when the PCM tubes are frozen (contracted). Some of the electricity produced could be used to control an external bladder or a motor to the tether line, such that depth cycling is continued for a very long period of time.

Alternatively, after the electricity is generated by the hydraulic motor, the exiting low-pressure oil from the hydraulic motor could be vented directly