Modular Integrated Stackable Layers (MISL)
MI_MSP430A Board Design Document (BDD)

Engineering Directorate
Avionic Systems Division

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Baseline
September 2013

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Lyndon B. Johnson Space Center
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Baseline	September 2013	Hester J. Yim	See Signature Page	Initial Release

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1. Introduction

This is a board-level design document for Modular Integrated Stackable Layers (MISL) MI_MSP430A board (P/N MSP430F5438A). The Board Design Document (BDD) contains the description, features of microcontroller, electrical and mechanical design, and drawings.

2. Description

MI_MSP430A board is designed based on an ultra low power microcontroller from Texas Instruments (TI) (P/N: MSP430F5438AIPZR) with an on-board Micro Secure Digital (SD) card slot (P6). It has two bus connectors to pass through power and genetic input/output signals. It also provides a Joint Test Action Group (JTAG) connector (P5) to program the flash embedded in microcontroller. (JTAG cable drawing is found in section 9).

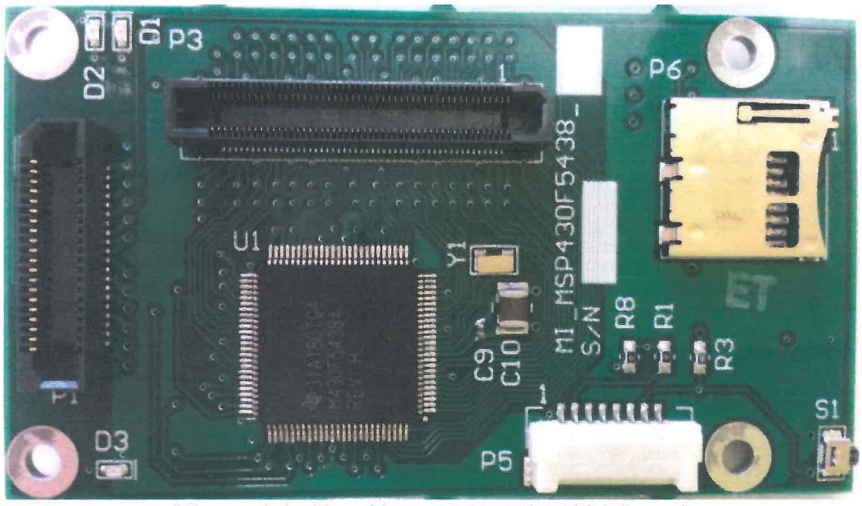


Figure 1.1 Top Side of MI_MSP430A board

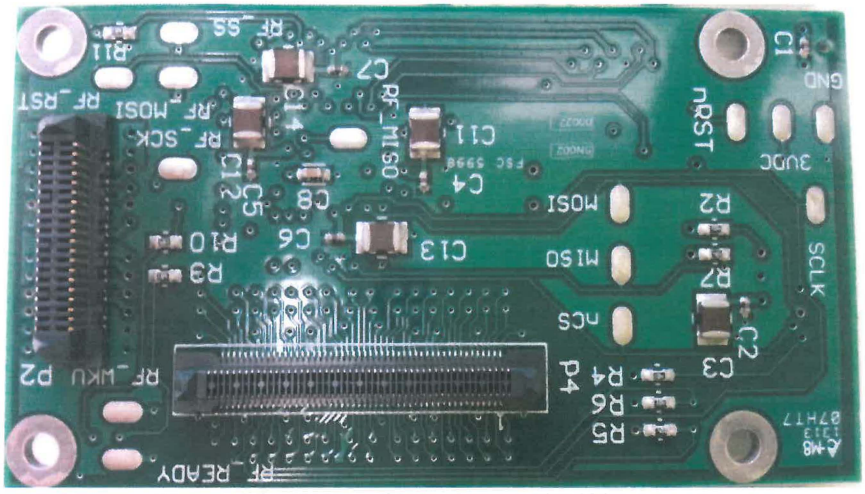


Figure 1.2 Bottom Side of MI_MSP430A board

3. Features

- Low Supply Voltage Range: 3.6 V Down to 1.8 V
- Ultralow Power Consumption
  - Active Mode (AM): All System Clocks Active
    230 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    110 µA/MHz at 8 MHz, 3.0 V, Random Access Memory (RAM) Program Execution (Typical)
  - Standby Mode:
    Real-Time Clock With Crystal , Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
    1.7 µA at 2.2 V, 2.1 µA at 3.0 V (Typical)
    Low-Power Oscillator, General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
    1.2 µA at 3.0 V (Typical)
  - Off Mode:
    Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up:
    1.2 µA at 3.0 V (Typical)
  - Shutdown Mode:
    0.1 µA at 3.0 V (Typical)
- Wake-Up From Standby Mode in 3.5 µs (Typical)
- 16-Bit Reduced Instruction Set Computing (RISC) Architecture
  - Extended Memory
  - Up to 25-MHz System Clock
- Flexible Power Management System
  - Fully Integrated Low Voltage Dropout (LDO) with Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power/Low-Frequency Internal Clock Source
  - Low-Frequency Trimmed Internal Reference Source
  - 32-kHz Crystals
  - High-Frequency Crystals up to 32 MHz
  - 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
  - 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
  - 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Up to Four Universal Serial Communication Interfaces
  - USCI_A0, USCI_A1, USCI_A2, and USCI_A3 Each Support Enhanced Universal Asynchronous Receiver/Transmitter (UART) supporting Auto-Baudrate Detection, IrDA Encoder and Decoder, Synchronous Schedule Performance Index (SPI)
  - USCI_B0, USCI_B1, USCI_B2, and USCI_B3 Each Support I^2C^{TM}, Synchronous SPI
- 12-Bit Analog-to-Digital (A/D) Converter
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - 14 External Channels, 2 Internal Channels
- Hardware Multiplier Supporting 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed

- Three Channel Internal Direct Memory Access (DMA)
- Basic Timer With Real-Time Clock Feature
- Operating temperature Ranges: -40°C to +85°C
- Radiation tolerant : Mean Time Between Upsets (MTBU) of 2360 days

Datasheet can be found in the TI Website: http://www.ti.com/product/msp430f5438a

4. Electrical Bus Connectors

4.1 Power Bus Connector

Power bus connector is used to supply voltages that are commonly used in low power systems. In general, a power bus connector on the bottom side of the board, P2, male, mates to a power supply board and a power bus connector on the top side of the board, P1, female, mates to any top stacking board to pass power lines. Pin 12, VTEST is tied ADC0 on MSP430A to provide a capability to monitor a chosen voltage (depending on the power supply board) if information is needed. The board is designed to use 3.0 Volts direct current (Vdc) from the power bus connector.

Table 1 Power Bus Connector Pin Assignment Table

Pin Number	Pin Name	MI_MSP430A Board, P1 & P2
1,3,5,8	5Vdc	Pass-Through
2, 4,6,7	5VGND	Pass-Through
9	1.8Vdc	Pass-Through
10	1V8GND	Pass-Through
11	2V5GND	Pass-Through
12	VTEST	VTEST_P6.0_PIN97
13	2.5Vdc	Pass-Through
14	3V3GND	Pass-Through
15,17,19,21	3VGND	3VGND
16,18,20,22	3.0Vdc	3.0Vdc
23,25,27,29	3.3Vdc	Pass-Through
24,26,28	3V3GND	Pass-Through
30,32	24VGND	Pass-Through
31,34	24Vdca	Pass-Through
33	Vusb	Pass-Through
35,37,39	9-36Vrtn	Pass-Through
36,38,40	9-36Vin	Pass-Through

4.2 Data Bus Connector

Data bus connector is used to connect all input/output (I/O) signals of MSP430A to be available to any communication and/or interface boards that are stacked up in a system. P4, a male connector footprint on the bottom side of the board, is not populated because there is no connection in a normal stack-up having a power board on the bottom. If needed, P4 can be used the same way as the P3, a female connector on top side.

Table 2 Data Bus Connector Pin Assignment Table

Pin Number	Pin Name	MI_MSP430A Board, P3 & P4
1	ADC_A0, GPIO	N/C (A0 tied to Vtest on Power bus)
2	ADC_A6, GPIO	P6.6_PIN3
3	ADC_A1, GPIO	P6.1_PIN98
4	ADC_A7, GPIO	P6.7_PIN4
5	ADC_A2, GPIO	P6.2_PIN99
6	ADC_A8, GPIO	P7.4_PIN5
7	ADC_A3, GPIO	P6.3_PIN100
8	ADC_A9, GPIO	P7.5_PIN6
9	ADC_A4, GPIO	P6.4_PIN1
10	ADC_A10, GPIO	P7.6_PIN7
11	ADC_A5, GPIO	P6.5_PIN2
12	ADC_A11, GPIO	P7.7_PIN8
13,14	AGND	AGND
15	ADC_A12, GPIO	N/C
16	ADC_A14, GPIO	N/C
17	ADC_A13, GPIO	N/C
18	ADC_A15, GPIO	N/C
19	GPIO_1	N/C
20	ADC_Vref+, GPIO	P5.0_PIN9
21	GPIO_2	N/C
22	ADC_Vref-, GPIO	P5.1_PIN10
23	GPIO_3	N/C
24	GPIO_33	P1.0_PIN17
25	GPIO_4	P8.7_PIN67
26	GPIO_34	P1.1_PIN18
27	GPIO_5	LED1_P9.6_PIN74
28	GPIO_35	P1.2_PIN19
29	GPIO_6	LED2_P9.7_PIN75
30	GPIO_36	P1.3_PIN20
31	GPIO_7	P10.6_PIN82
32	GPIO_37	P1.4_PIN21
33	GPIO_8	P10.7_PIN83
34	GPIO_38	P1.5_PIN22
35	GPIO_9_SENA_SCLK	P9.0_PIN68
36	GPIO_39_CLK	P1.6_PIN23
37	GPIO_10_SIMO_SDA	P9.1_PIN69
38	GND	GND
39	GPIO_11_SOMI_SCL	P9.2_PIN70
40	GPIO_40_CLK	P2.0_PIN25
41	GPIO_12_SCLK_SENA	P9.3_PIN71
42	GPIO_41	P2.1_PIN26
43	GPIO_13_TXD_SIMO	P9.4_PIN72
44	GPIO_42	P2.2_PIN27
45	GPIO_14_RXD_SOMI	P9.5_PIN73
46	GPIO_43	P2.3_PIN28
47	GPIO_15_SENA_SCLK	RF_SS_P10.0_PIN76
48	GPIO_45_CLK	P2.4_PIN29
49	GPIO_16_SIMO_SDA	RF_MOSI_P10.1_PIN77
50	GPIO_46_CLK	P2.6_PIN31
51	GPIO_17_SOMI_SCL	RF_MISO_P10.2_PIN78
52	GPIO_47	P2.7_PIN32

53	GND	GND
54	GPIO_48	P4.0_PIN43
55	GPIO_18_SCLK_SENA	RF_SCK_P10.3_PIN79
56	GPIO_49	P4.1_PIN44
57	GPIO_19_TXD_SIMO	LED3_P10.4_PIN80
58	GPIO_50	P4.2_PIN45
59	GPIO_20_RXD_SOMI	RF_RST_P10.5_PIN81
60	GPIO_51	P4.3_PIN46
61	GPIO_44	RF_READY_P2.5_PIN30
62	GPIO_52	P4.4_PIN47
63	GPIO_21_SENA_SCLK	P3.6_PIN41
64	GPIO_53	P4.5_PIN48
65	GPIO_22_SIMO_SDA	P3.7_PIN42
66	GPIO_54	P4.6_PIN49
67	GPIO_23_SOMI_SCL	P5.4_PIN51
68	GPIO_55_CLK	P4.7_PIN50
69	GPIO_24_SCLK_SENA	P5.5_PIN52
70	GND	GND
71	GPIO_25_TXD_SIMO	P5.6_PIN53
72	GPIO_56_CLK	P11.0_PIN84
73	GPIO_26_RXD_SOMI	P5.7_PIN54
74	GPIO_57_CLK	P11.1_PIN85
75	GPIO_27_SENA_SCLK	RF_WKU_P3.0_PIN33
76	GPIO_58_CLK	P11.2_PIN86
77	GPIO_28_SIMO_SDA	MOSI_P3.1_PIN34 (uSD)
78	GPIO_59	P8.0_PIN57
79	GPIO_29_SOMI_SCL	MISO_P3.2_PIN35 (uSD)
80	GPIO_60	P8.1_PIN58
81	GND	GND
82	GPIO_61	P8.2_PIN59
83	GPIO_30_SCLK_SENA	SCLK_P3.3_PIN36 (uSD)
84	GPIO_62	P8.3_PIN60
85	GPIO_31_TXD_SIMO	NCS_P3.4_PIN39 (uSD)
86	GPIO_63	P8.4_PIN61
87	GPIO_32_RXD_SOMI	P3.5_PIN40
88	GPIO_64	P8.5_PIN65
89	JTAG_TDO	JTAG_TDO
90	GPIO_65	P8.6_PIN66
91	STACK_TDI1	JTAG_TDI1
92	GPIO_66	P7.3_PIN56
93	STACK_TDI2	JTAG_TDI2
94	GPIO_67	P7.2_PIN55
95	JTAG_TMS	TMS_PJ.2_PIN94
96	GPIO_68_XTIN	P5.2_PIN89
97	JTAG_TCK	TCK_PJ.3_PIN95
98	GPIO_69_XTOUT	P5.3_PIN90
99	nRESET	NRST_PIN96
100	TEST	TEST_PIN91

5. Mechanical

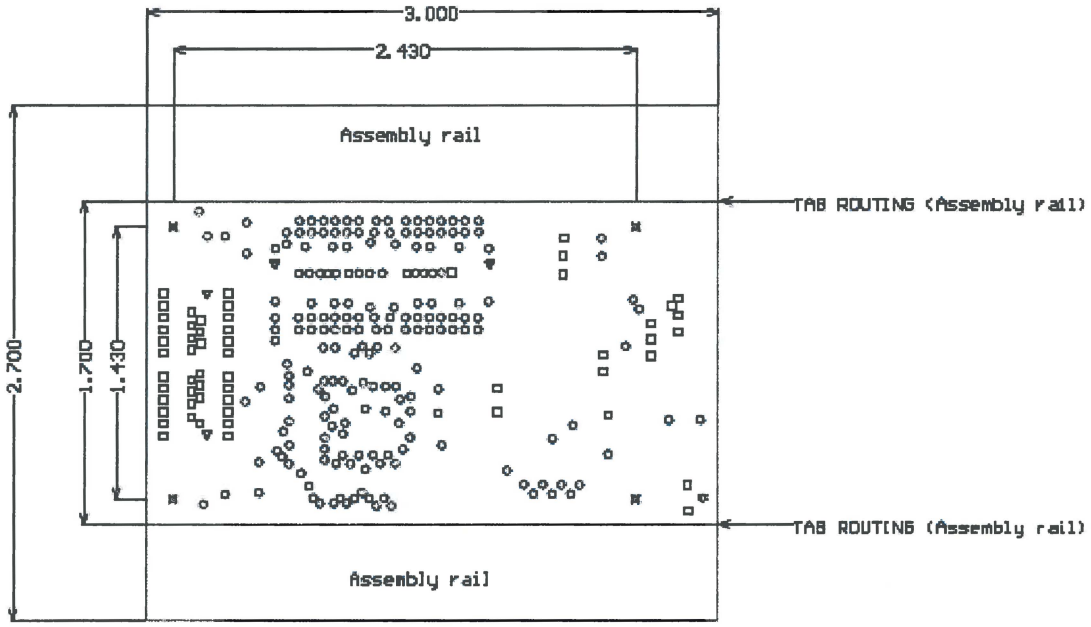


Figure 5.1 Assembly Rail

Layer Stack Up Detail for: ModularProcessor.PcbDoc

Layer Name	Barber Document	Copper Thickness	Dielectric Height	Dielectric Material
Top Solder Mask	(.GTS)		0.4mil	Solder Resist
Top Layer	(.GTL)	1.4mil		
			5MIL +- .8MIL	FR-4
Internal Plane 1	(.GP1)	1.4mil		
			5mil +- .8MIL	FR-4
Mid-Layer 1	(.G1)	1.4mil		
			35mil NOM	FR-4
Mid-Layer 4	(.G2)	1.4mil		
			5mil +- .8MIL	FR-4
Internal Plane 2	(.GP2)	1.4mil		
			5mil +- .8MIL	FR-4
Bottom Layer	(.GBL)	1.4mil		
Bottom Solder Mask	(.GBS)		0.4mil	Solder Resist

NOM BOARD THK .062 IN

Figure 5.2 Layer Stack Up Detail for Modular Processor

6. Bill of Materials

Table 3 Bill of Materials

	Designator	Manufacturer Part Number	Manufacturer	Component Link1 URL	Description	Populate
1	C1, C2, C4, C5, C6, C7, C9	C0402C104K8PACTU	Kemet	http://www.kemet.com/datasheets&C0402C104K8PACTU	CAP .10UF 10V CERAMIC X5R 0402	Yes
2	C3, C10, C11, C12, C13, C14	GRM329F51A106ZA01D	Murata Electronics North America	http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/GRM329F51A106ZA01.pdf	CAP CERM 10UF 10% 10V X7R 1210	Yes
3	C8	GRM188R71E474KA12D	Murata Electronics North America	http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/GRM188R71E474KA12.pdf	CAP CER .47UF 25V X7R 0603	Yes
4	D1	LTST-C190GKT	Lite-On Inc	http://media.digikey.com/pdf/Data%20Sheets/Lite-On%20PDFs/LTST-C190GKT.pdf	LED GREEN CLEAR 0603 SMD	Yes
5	D2	LTST-C190YKT	Lite-On Inc	http://media.digikey.com/pdf/Data%20Sheets/Lite-On%20PDFs/LTST-C190YKT.pdf	LED YELLOW CLEAR 0603 SMD	Yes
6	D3	LTST-C191KRKT	Lite-On Inc	http://optoelectronics.liteon.com/en-us/api/DwonloadFileHandler.ashx?txtSpecNo=DS22-2000-223&txtPartNo=LTST-C191KRKT	LED SUPER RED CLR THIN 0603 SMD	Yes
7	P1	ERF8-020-05.0-S-DV-TR	Samtec Inc	http://www.samtec.com/ftppub/pdf/erf8.pdf	CONN RCPT 40POS 0.8MM GOLD SMD	Yes
8	P2	ERM8-020-02.0-S-DV-TR	Samtec Inc	http://www.samtec.com/ftppub/pdf/erm8.pdf	CONN HEADER 40POS 0.8MM GOLD	Yes
9	P3	ERF5-050-05.0-L-DV-TR	Samtec Inc	http://www.samtec.com/ftppub/pdf/erf8.pdf	CONN RCPT 100POS 0.8MM GOLD SMD	Yes
10	P4	ERM5-050-05.0-S-DV-K-TR	Samtec Inc	http://www.samtec.com/ftppub/pdf/erm8.pdf	CONN HEADER 100POS 0.8MM GOLD	No
11	P5	DF14-8P-1.25H(56)	Hirose Electric Co Ltd	http://www.hirose.co.jp/cataloge_hp/e53800017.pdf	CONN HEADER 8POS 1.25MM R/A SMD	Yes

12	P6	500873-0806	Molex Connector Corporation	http://www.molex.com/pdm_docs/sd/5008730806_sd.pdf	CONN TRANSFLSH R/A PUSH-PUSH SMD	Yes
13	R1, R8	ERJ-3GEY0R00V	Panasonic - ECG	http://industrial.panasonic.com/www-cgi/jvcr13pz.cgi?E+PZ+3+AOA0001+ERJ3GEY0R00V+7+WW	RES 0.0 OHM 1/10W 0603 SMD	R1(Yes), R8 (No)
14	R2, R3, R4, R5, R6, R7	ERJ-3GEYJ104V	Panasonic - ECG	http://industrial.panasonic.com/www-cgi/jvcr13pz.cgi?E+PZ+3+AOA0001+ERJ3GEYJ104V+7+WW	RES 100K OHM 1/10W 5% 0603 SMD	Yes
15	R9, R10, R11	ERJ-3GEYJ681V	Panasonic - ECG	http://industrial.panasonic.com/www-cgi/jvcr13pz.cgi?E+PZ+3+AOA0001+ERJ3GEYJ681V+7+WW	RES 680 OHM 1/10W 5% 0603 SMD	Yes
16	S1	B3U-3000P-B	Omron Electronics Inc-EMC Div	http://components.omron.com/components/web/pdflib.nsf/0/2DD3893C7DD33E9E862572900079E9D6/$file/B3U_1110.pdf	TACTILE SIDE ACTUATED W/BOSS	Yes
17	U1	MSP430F5438AIPZ	Texas Instruments	http://focus.ti.com/lit/ds/symlink/msp430f5438.pdf	IC MCU 16BIT 256K FLASH 100-LQFP	Yes
18	Y1	ABS07-32.768KHZ-9-T	Abracon Corporation	http://www.abracon.com/Resonators/ABS07.pdf	CRYSTAL 32.768KHZ 9PF SMD	Yes

7. Schematics

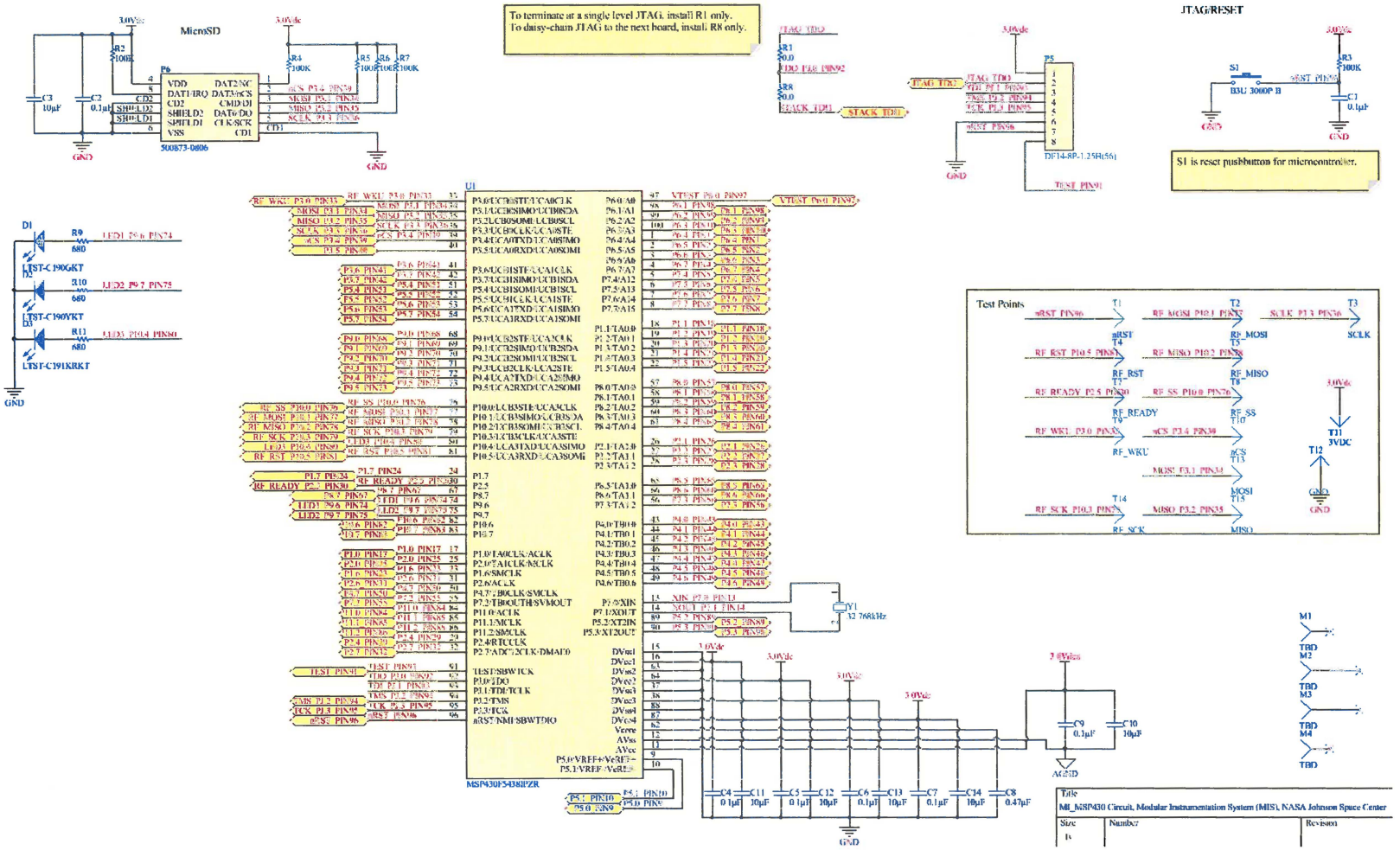
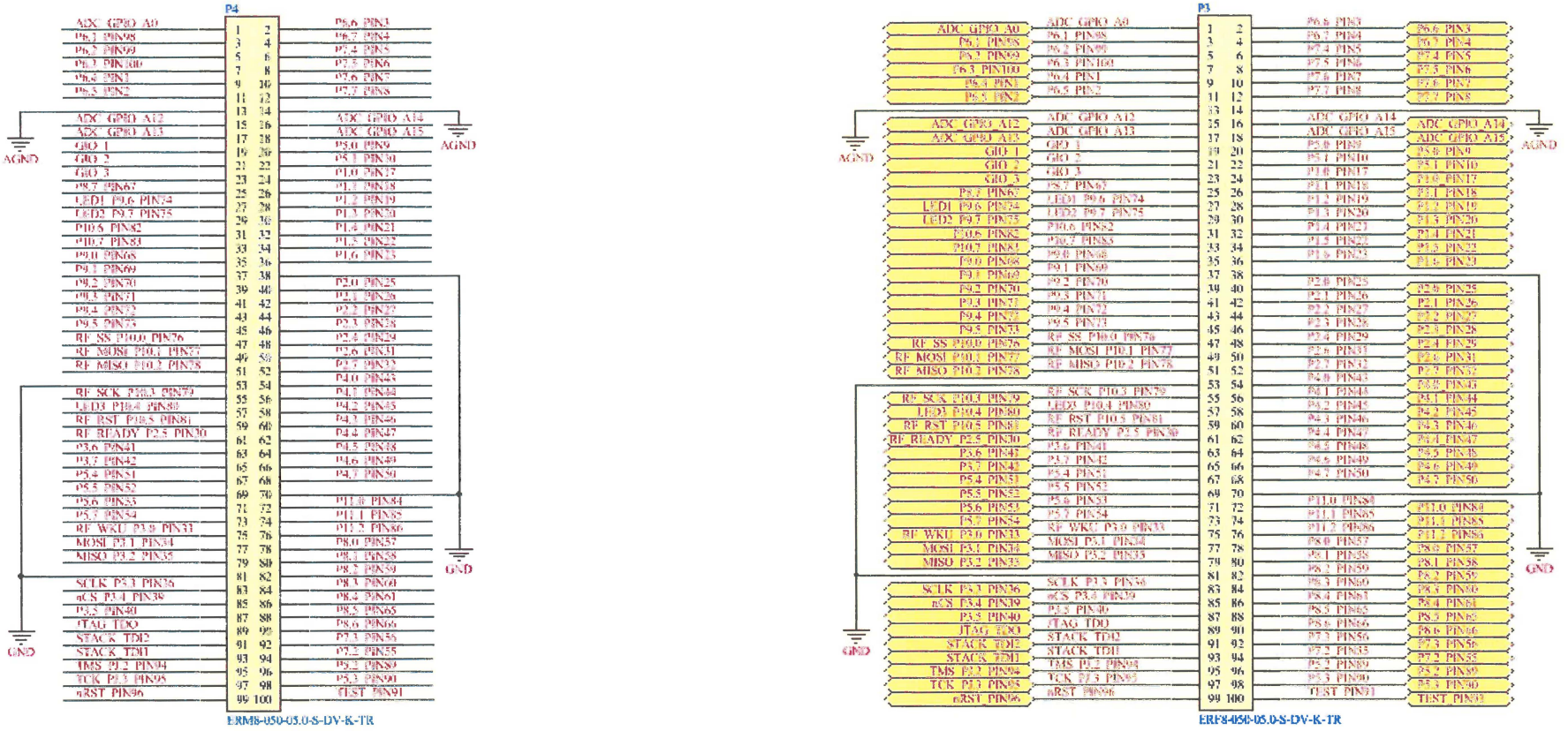
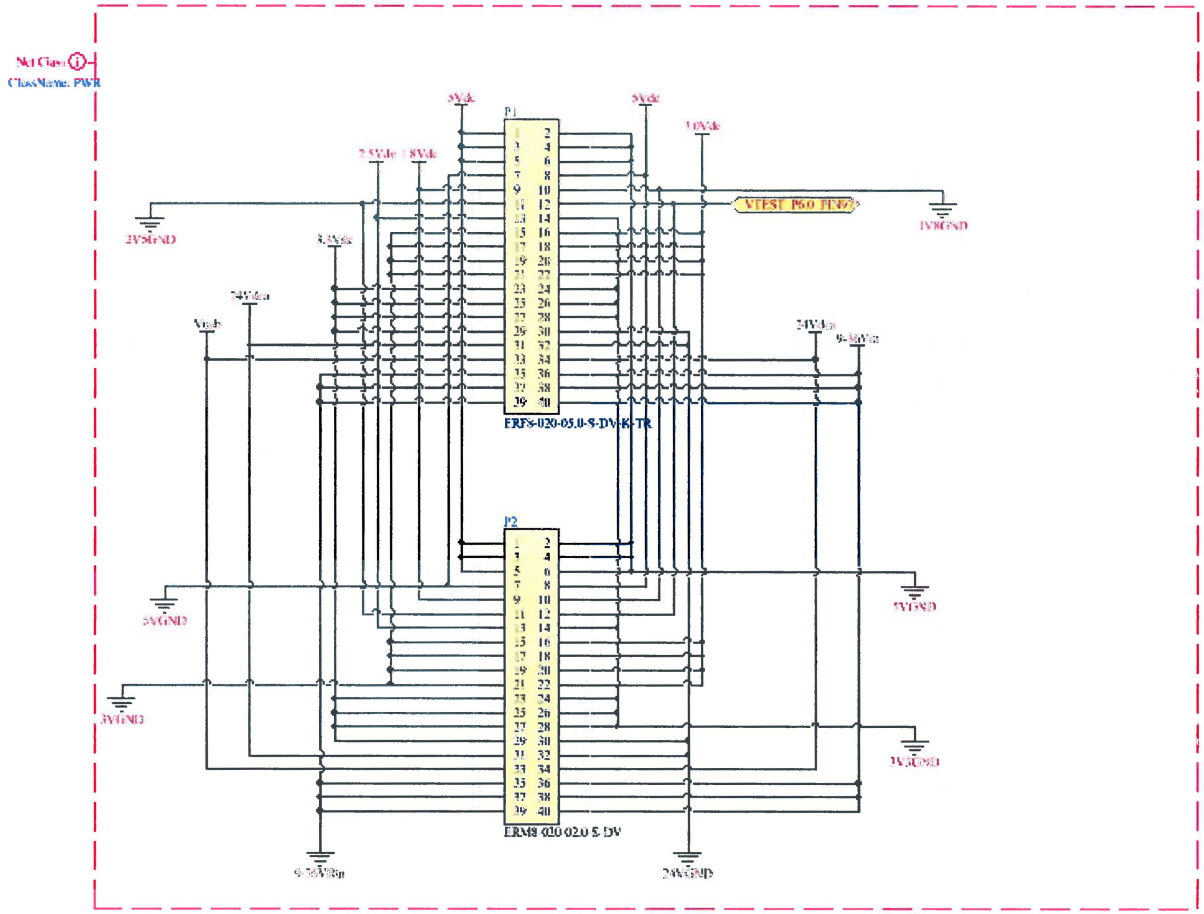


Figure 7.1 MSP430A Schematic



Place ERM part on the bottom side and ERF part on the top side

Figure 7.2 Data Bus Schematic



ERM connectors on Bottom Layer, ERF connectors on the Top Layer

Figure 7.3 Power Bus Schematic

8. Top and Bottom Silkscreen

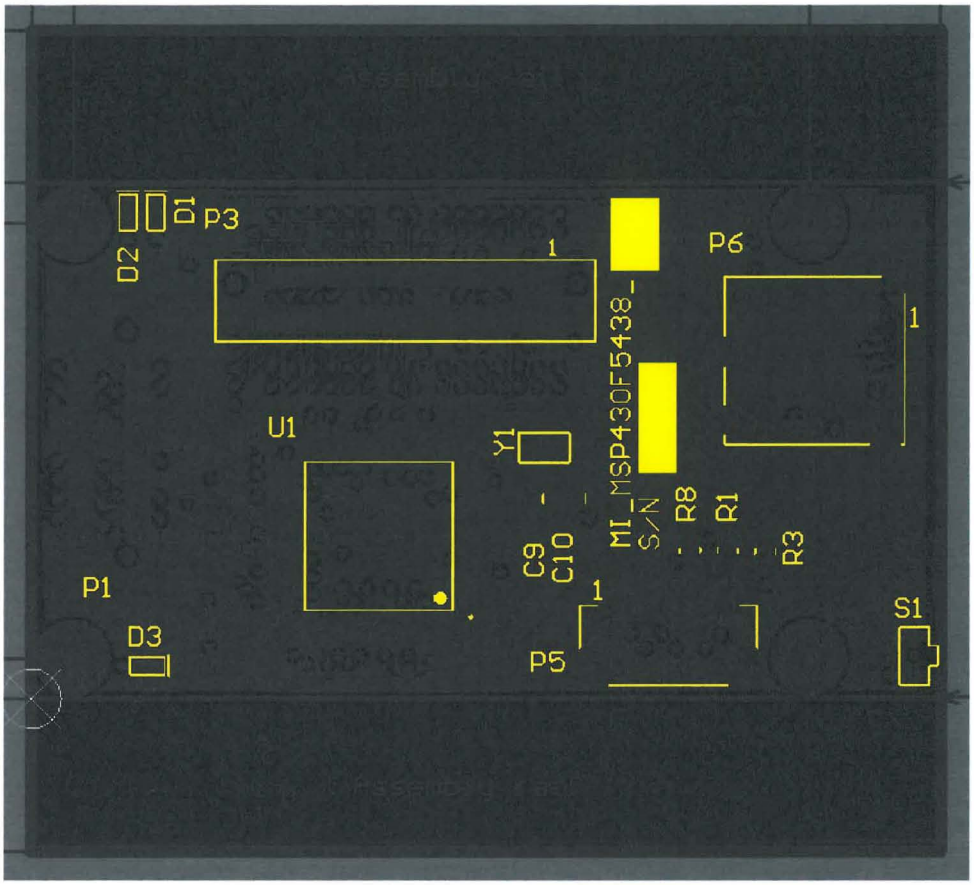


Figure 8.1 Top Silkscreen

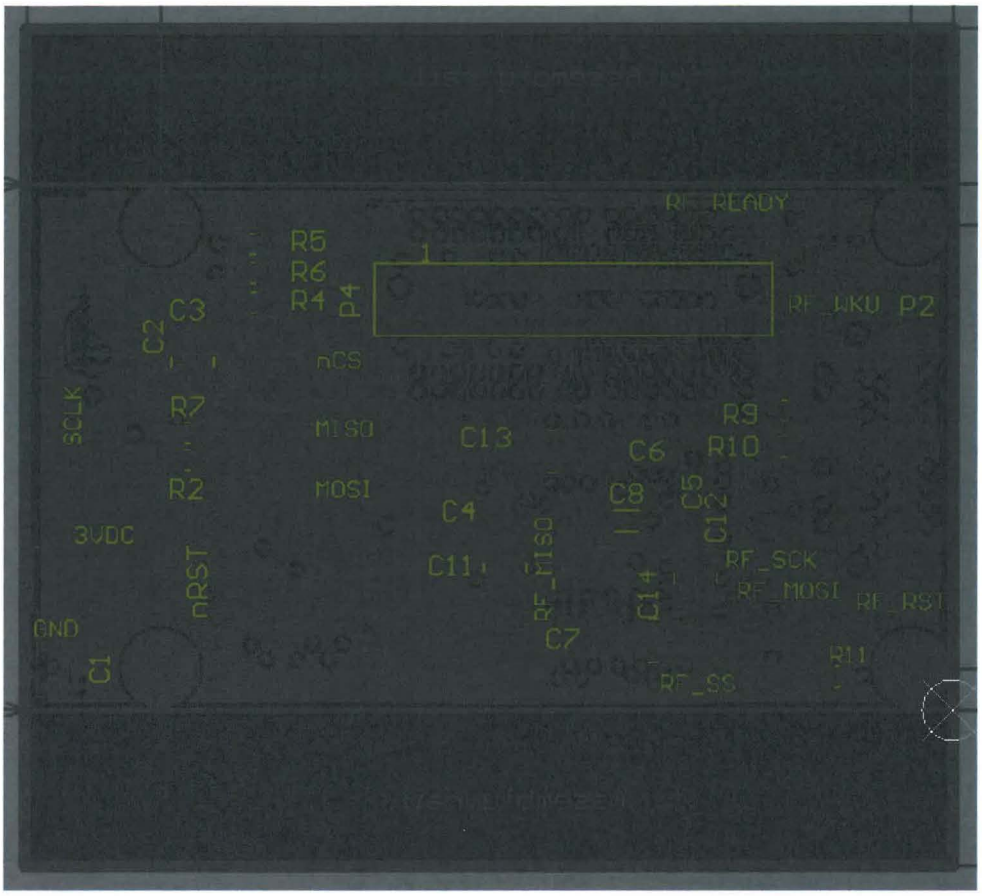


Figure 8.2 Bottom Silkscreen

9. JTAG Cable Drawing

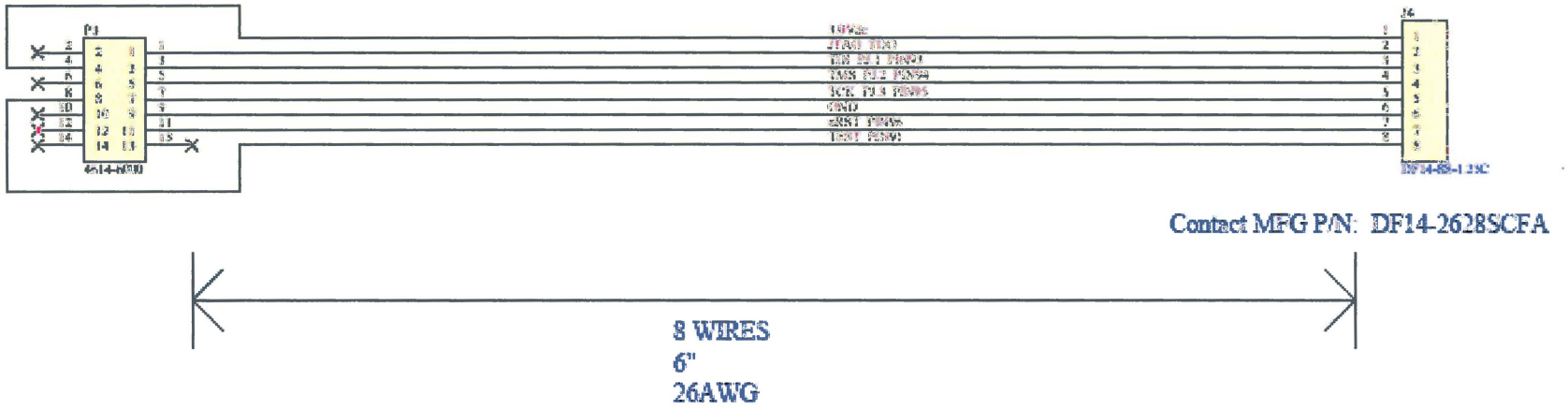


Figure 9.1 JTAG Cable Drawing

Appendix A - Acronym List

AM	Active Mode
ADC	Analog Digital Converter
A/D	Analog-to-Digital
BDD	Board Design Document
C	Celsius
C&DH	Command and Data Handling
DMA	Direct Memory Access
EHDC	External High Definition Camera
EV	Command and Data Handling Branch
ISS	International Space Station
I/O	Input/Output
JSC	Johnson Space Center
JTAG	Joint Test Action Group
LDO	Low Voltage Dropout
MISL	Modular Integrated Stackable Layers
MHz	Megahertz
MTBU	Mean Time Between Upsets
NASA	National Aeronautics and Space Administration
P/N	Part Number
RAM	Random Access Memory
SD	Secure Digital
SPI	Schedule Performance Index
TI	Texas Instruments
µA	Microampere
UART	Universal Asynchronous Receiver/Transmitter
V	Volts
Vdc	Volts Direct Current

Appendix B - Supporting Data