All-Digital Baseband 65nm PLL/FPLL Clock Multiplier using 10-cell Library

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Robert L. Shuler, Jr.[1], Qiong Wu[2], Rui Liu[3] and Li Chen[4]

[1]robert@mc1soft.com – robert.l.shuler@nasa.gov
NASA Johnson Space Center EV5
2101 NASA Parkway, Houston, TX 77058

[2]qiong.we@usask.ca
[3]rul070@mail.usask.ca
[4]lic900@campus.usask.ca
Department of Electrical and Computer Engineering
University of Saskatchewan
57 Campus Drive, Saskatoon, Saskatchewan, S7N 5A9, Canada

INTRODUCTION

PLLs for clock generation are essential for modern circuits, to generate specialized frequencies for many interfaces and high frequencies for chip internal operation. These circuits depend on analog circuits and careful tailoring for each new process, and making them fault tolerant is an incompletely solved problem. Until now, all digital PLLs have been restricted to sampled data DSP techniques and not available for the highest frequency baseband applications.

This paper presents the design and preliminary evaluation of an all-digital baseband technique built entirely with an easily portable 10-cell digital library. The library is also described, as it aids in research and low volume design porting to new processes.

The advantages of the digital approach are the wide variety of techniques available to give varying degrees of fault tolerance, and the simplicity of porting the design to new processes, even to exotic processes that may not have analog capability. The only tuning parameter is digital gate delay.

An all-digital approach presents unique problems and standard analog loop stability design criteria cannot be directly used. Because of the quantization of frequency, there is effectively infinite gain for very small loop error feedback. The numerically controlled oscillator (NCO) based on a tapped delay line cannot be reliably updated while a pulse is active in the delay line, and ordinarily does not have enough frequency resolution for a low-jitter output.

NCO

We present two approaches to these various problems. Both approaches use an NCO which has four phases of output resolution between each tap. The 6-bit tap mux with the 2-bit output phase selector gives an 8-bit or 512 step variable delay which can generate frequencies between 75 and 400 MHz. The resolution provides about 5% frequency resolution at the high end and 1% at the low end. A block diagram of the tapped delay is shown in Figure 1. Two gates are used for each delay (not shown) in order to avoid alternating pulse polarity issues. The 4-phase output select, tuned with capacitance of gate loads, provides half a gate delay resolution.

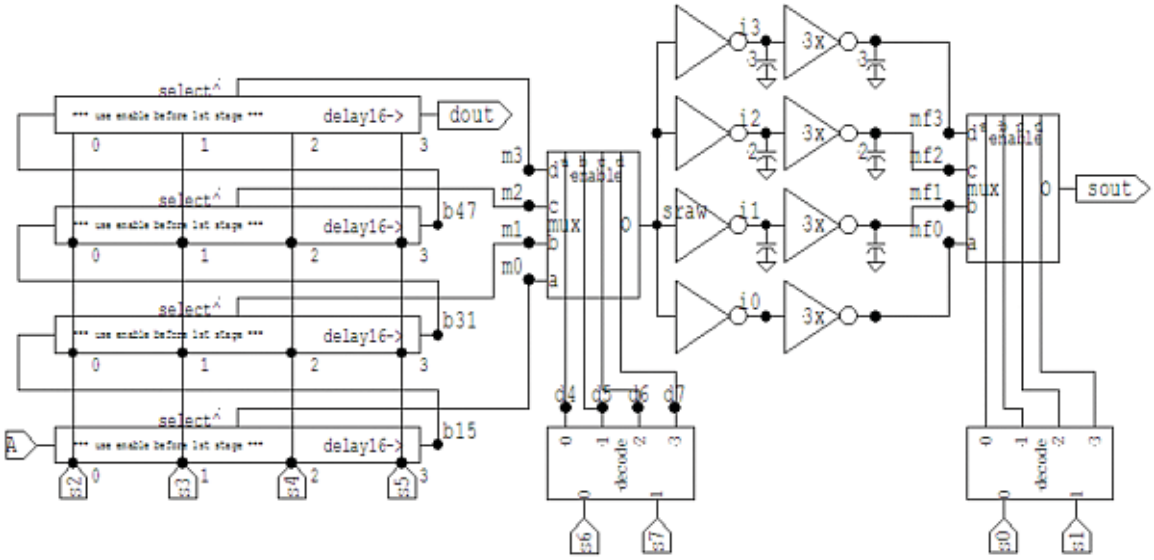

Fig. 1 – 64 tap delay line with 4-phase output select

ON-CHIP FPLL LOOP

The first approach uses an on-chip control loop which combines frequency and phase feedback. Counters are provided for the input signal (always a count of 2) and output signal (4, 5, 8 and 16) and by comparing the rate of counter outputs and making them equal, frequency multiplication of 2x, 2.5x, 4x and 8x is obtained. Frequency and phase detectors operate on the counter signals and the raw clock signals respectively, shown in Figure 2.

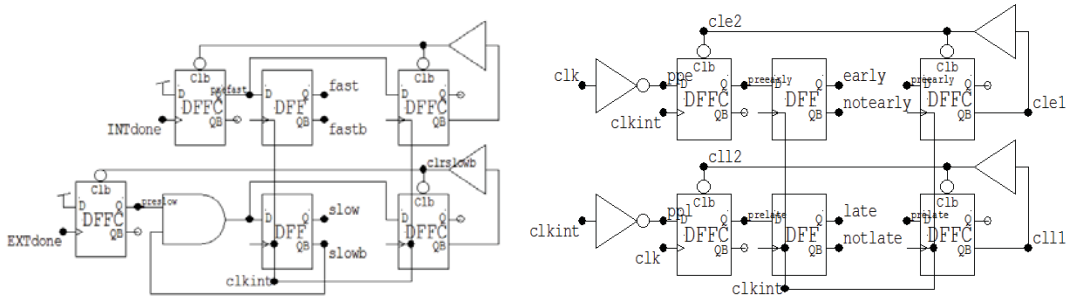

Fig. 2 – Frequency (left) and Phase Detectors

When the frequency detector generates a fast or slow signal (non-simultaneous arrival of internal and external clocks within an interval of one internal clock cycle) the delay tap is incremented or decremented appropriately. Speed of convergence was sacrificed for simplicity in the internal control loops.

When there is no adjustment needed for frequency, the phase loop is allowed to control. Ideally the phase control could have been done with temporary adjustment of the delay taps, but again for simplicity a separate one-time phase adjustment circuit was provided which will be detailed in the full paper. This frequency-phase strategy avoids a lot of control loop jitter which would otherwise occur due to the delays and quantizations inherent in an all-digital pure PLL strategy.

Phase adjustment was disabled for the fractional multiplier of 2.5x because of lack of time in the development cycle to devise logic to reliably anticipate when a comparison edge for the 2.5x would be available, so it provides frequency lock only. Table 1 gives the measured results of lock frequencies for the internal control loop.

Mult	lowest lock	highest	output	notes……
2x	37 MHz	n/a*	74 MHz	*signal gen limited to 52.5 MHz
2.5x	32 MHz	n/a	80 MHz	frequency lock only, by design
4x	18.8 MHz	n/a	75.2 MHz	some jitter over 36 MHz input
8x	9.2 MHz	46.6 MHz	73.6-372.8	

A typical output is shown in Figure 3.

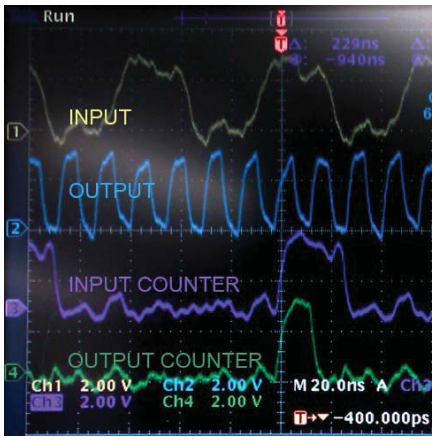

Fig. 3 – 4x lock

Some jitter was inevitable for frequencies over about 144 MHz on the output because the phase adjustment granularity is 4x less than the tapped delay line granularity for about a 20% short term frequency variation at those frequencies. A more sophisticated design using the tapped delay for phase adjustment should reduce this problem.

OFF-CHIP FPGA CONTROL

An open loop mode is provided with NCO increment/decrement control so that an external FPGA can be used to control the NCO, monitor input and output frequencies, and implement various more sophisticated algorithms. These have not yet been implemented, but the candidates include:

- More rapid convergence
- Limitations on re-convergence once frequency lock is required
- Experimental techniques for pure PLL operation

Interfaces for two FPGA boards are being developed, and would-be collaborators may be able to obtain access to one of the several development boards to test their own strategies.

RESULTS

The on-chip circuits, both NCO and control loop, are implemented in TMR, and if time can be borrowed from another run (which is a possibility but not a certainty), then heavy ion test data will be available. More detailed descriptions of stability and of alternate external algorithms will also be presented.