

High-Speed On-Board Data Processing for Science Instruments

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ABSTRACT

A new development of on-board data processing platform has been in progress at NASA Langley Research Center since April, 2012, and the overall review of such work is presented in this paper. The project is called High-Speed On-Board Data Processing for Science Instruments (HOPS) and focuses on a high-speed scalable data processing platform for three particular National Research Council's Decadal Survey missions such as Active Sensing of CO₂ Emissions over Nights, Days, and Seasons (ASCENDS), Aerosol-Cloud-Ecosystems (ACE), and Doppler Aerosol Wind Lidar (DAWN) 3-D Winds. HOPS utilizes advanced general purpose computing with Field Programmable Gate Array (FPGA) based algorithm implementation techniques. The significance of HOPS is to enable high speed on-board data processing for current and future science missions with its reconfigurable and scalable data processing platform. A single HOPS processing board is expected to provide approximately 66 times faster data processing speed for ASCENDS, more than 70% reduction in both power and weight, and about two orders of cost reduction compared to the state-of-the-art (SOA) on-board data processing system. Such benchmark predictions are based on the data when HOPS was originally proposed in August, 2011. The details of these improvement measures are also presented. The two facets of HOPS development are identifying the most computationally intensive algorithm segments of each mission and implementing them in a FPGA-based data processing board. A general introduction of such facets is also the purpose of this paper.

Keywords: onboard, high speed, FPGA, DAWN, ACE, ASCENDS

1. INTRODUCTION

High-Speed On-Board Data Processing for Science Instruments (HOPS) at NASA Langley Research Center (LaRC) is a 3-year project funded by the NASA's Earth Science Technology Office (ESTO) Advanced Information Systems Technology (AIST) program. The project period is April 1st, 2012 through March 31st, 2015. The goal of HOPS is to develop a high-speed on-board reconfigurable and scalable data processing platform for science instruments. HOPS will support the three missions from the National Research Council's (NRC) Decadal Survey (DS) of Earth Science and Applications from Space [1]: ASCENDS (Active Sensing of CO₂ Emissions over Nights, Days, and Seasons) [2-9], 3-D Winds, and ACE (Aerosol Cloud Ecosystems). The project DAWN (Doppler Aerosol Wind Lidar) is chosen for the 3-D Winds category. The entry and the exit technical readiness levels (TRLs) are 2 and 5, respectively. This paper presents an overview of HOPS including the uniqueness, target technical specifications, and the summary of the latest development.

2. UNIQUENESS AND SIGNIFICANCE OF HOPS

The keys to high-speed on-board data processing are high-speed computation elements, sufficient memory to hold intermediate values, and sufficient bandwidth between the computation elements and the memory. The latest general purpose processors (GPPs) and digital signal processors (DSPs) do not satisfy them simultaneously, but the reprogrammable Field Programmable Gate Arrays (FPGAs) offer the feasibility of meeting all aspects by implementing

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the high speed computation elements in the FPGA [10]. Designs developed at LaRC such as reconfigurable scalable computing (RSC) [12] and SpaceCube 2.0 [13] are being considered to be leveraged for the development of HOPS boards.

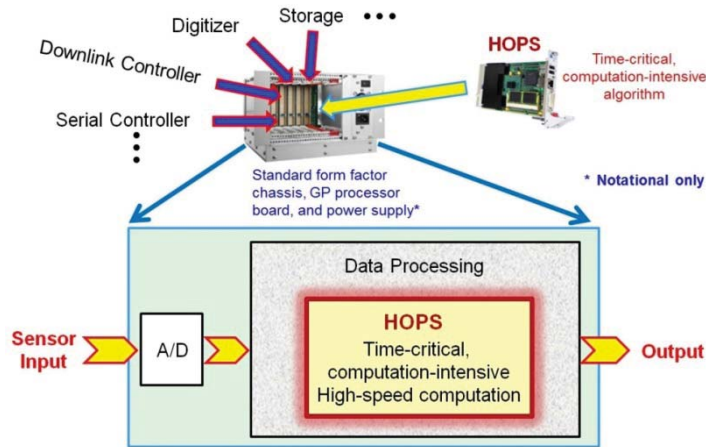


Figure 1 HOPS is an enabler. HOPS does not take over the entire data processing but replace the most computationally intensive part of it so that the project can process the data real-time.

HOPS is an enabler for science mission with extremely high data processing rate. Currently, no commercially off-the-shelf (COTS) board offers the specifications that HOPS is targeting to achieve. The FPGA/memory bandwidth of HOPS is approaching 16 GB/sec, and the inner-board bandwidth of HOPS is approaching 4 GB/sec. HOPS is adaptable with quick turn-around time since the high-speed computation elements can be reused with extremely high memory and inter-board bandwidths and plug and play computing architecture. The SystemC IP modules and VHDL IP modules are all reusable.

The current SOA GPP boards in spaceborne data processing is up to one GHz [14]. For an equivalent net performance and first order comparison, it is anticipated that there will be two orders of magnitude improvement with HOPS in size, mass, power, volume and cost when compared to a single core GHz GPP board solution.

	Downlink all data	SOA Radiation Tolerant 1 GHz GPP PowerPC 750FX	SOA Radiation Tolerant DSP SMJ320C6701-SP	HOPS
FFT Count/sec	N/A	91	4	6,096
Computation Board Qty for FFT	N/A	51	1,145	1
Power (Watt)	N/A	612	13,740	12
Mass (lb.)	N/A	35.19	790.05	0.69
Hardware Cost	N/A	\$10.2 Million	\$229 Million	\$200 K
Downlink Data Volume (Mbps)	640	< 20	< 20	< 20

Table 1 Superior performance indices of HOPS compared to the SOA Technologies

As for top fast Fourier transform (FFT) performance benchmarks using 65,536 (2^{16})-point single precision floating point FFT as in ASCENDS algorithms, a single SOA Radiation tolerant 1 GHz GPP Power PC 750 FX board would perform 91 executions/sec, whereas a single HOPS processing board will offer 6,096 executions/sec, almost 66 times faster.

HOPS employs path-to-flight technology and will follow flight board design rules. All components of HOPS boards will have flight equivalent parts; however, this does not imply directly swappable components. Customization will be

necessary, but not as in a starting from scratch way. Since HOPS will have common IP cores, the HOPS boards will have reusable user-friendly computation elements and allow quick algorithm implementation and easy adjustments. Since HOPS is based on modular board design concept with FPGAs, HOPS boards will be scalable and reconfigurable. The form factor of HOPS is compact PCI (cPCI), and the cPCI bus will be for slower tasks.

3. SYNERGY WITH NASA MISSIONS

HOPS is fully scalable and can be reconfigured with minimal or no additional efforts for other applications that require extensive real-time data processing and a high processing rate. HOPS will enable ASCENDS to execute more sophisticated and computationally intensive data processing algorithms in real-time while reducing data bandwidth downlink and improving data quality. HOPS will allow faster lidar pulse rates with a larger FFT size to increase the resolution in real-time wind profiling. HOPS will benefit ACE by significantly reducing the data latency allowing real-time cloud profiles. HOPS can also make a pixel-based image processing algorithm possible in real-time for the Autonomous Landing and Hazard Avoidance Technology (ALHAT) [11]. As for ASCENDS, HOPS replaces time domain data processing with frequency domain processing via 64K-long FFTs and as a result a real-time data processing will become possible. ASCENDS may use HOPS boards for its flight campaign on the Global Hawk.

	Data in Sample Counts	Data Out Sample Counts *	Reduction Rate	
ASCENDS	8,388,608 **	24	99.99%	In = 64K @ 64 Hz, 2 ch Out = 12 ratios, 2 ch
3-D Winds (DAWN)	1,310,720	200	99.98%	In = 64K @ 20 Hz Out = 200 peaks
ACE	40,000	400	99%	In = 400 @ 100 Hz Out = 400 averages

Table 2 Application of HOPS to select DS missions. *Excluding raw data archive (infrequent, good-to-have feature). **Twice the ASCENDS airborne requirement which is 4 Million Samples (MS) per second (2 MS/channel, 2 channels total). 13,107,200 samples at 100 Hz have tested successfully. HOPS COTS data processing rate is far greater. (at least 20 MS/sec for two channels)

Table 2 shows the data reduction rate of the three DS missions with HOPS. The table accounts for only essential and meaningful science data products for further processing. HOPS is reconfigurable and can be reprogramed if algorithm needs to change for different science needs.

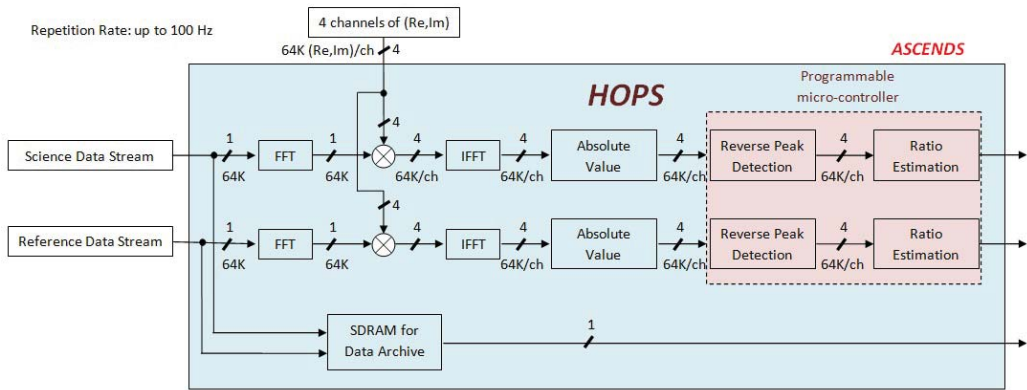


Figure 2 Algorithm of ASCENDS for HOPS (most computationally intensive part).

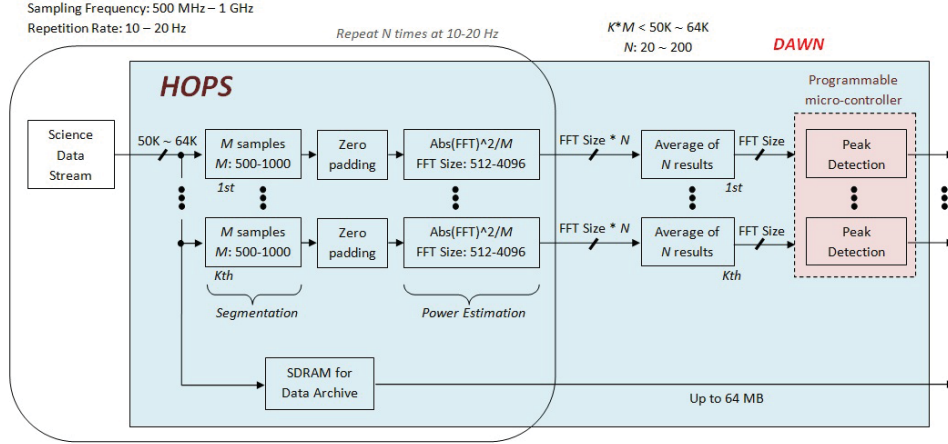


Figure 3 Algorithm of 3D-Winds for HOPS (most computationally intensive part).

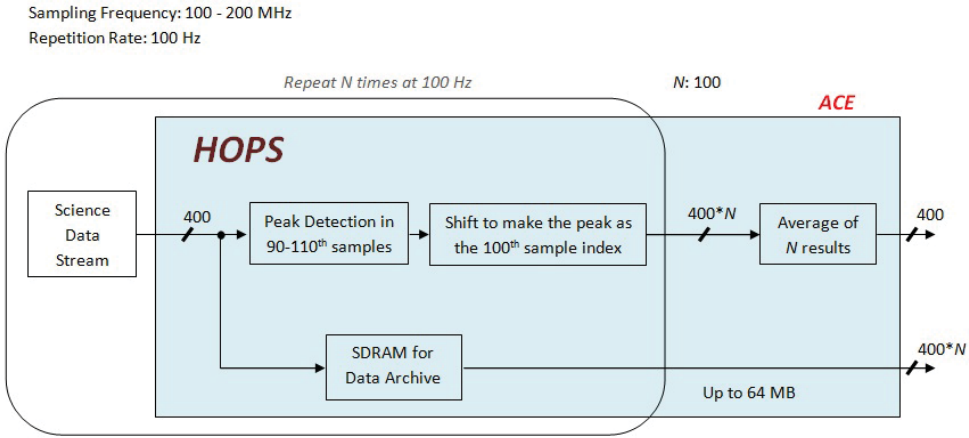


Figure 4 Algorithm of ACE for HOPS (most computationally intensive part).

Figures 2 – 4 depict the abstract description of the algorithms to be implemented on HOPS for ASCENDS, 3-D Winds, and ACE. The challenge with ASCENDS is the length of FFT and how often such calculations must be made. 3-D Winds imposes challenges of more complicated data processing routines, and implementation of variable parameters. ACE may require additional sophisticated signal processing routines to be implemented such as adaptive Kalman filtering.

4. DEVELOPMENT OF HOPS

The development of HOPS is tri-fold. First, candidate algorithms that are time critical and most computationally intensive will be identified for ASCENDS, 3-D Winds, and ACE. Such algorithms will be analyzed for parallel implementation and the HOPS computing architecture will be designed. This is done in SystemC that simulates the computation elements and their performance and timing. Second, a HOPS prototype system (HOPS COTS) is built based on the computing architecture in SystemC using COTS components. VHDL codes are also developed for the FPGAs. The HOPS COTS employs Xilinx Virtex 6. Once the FPGA IP Cores are ready, the HOPS COTS is tested in a lab environment. All performance specification of HOPS are tested and validated by analysis and demonstration and the science requirements of projects are ensured to be met. Lastly, the final HOPS custom board is built based on the HOPS COTS and its testing. The entry TRL is 2 and the exit TRL is expected to be 5.

5. STATUS QUO

The software model of HOPS was designed in SystemC, which is a set of C++ classes and macros offering an event-driven simulation kernel in C++ environment. The computationally intensive parts of ASCENDS and 3-D Winds data processing algorithms have been identified for HOPS. Such algorithms also have been implemented in another software package such as LabVIEW and the science products from the HOPS software model in both SystemC and LabVIEW have been compared for accuracy tests. The difference between the two software models was almost negligible and within the tolerance level required by the projects. The difference is attributed to the fact that the HOPS SystemC's calculation was in IEEE single precision floating point while the LabVIEW's calculation was in IEEE double precision floating point. The time domain data processing of ASCENDS was modified to run in the frequency domain using the FFT in order to improve the processing speed without losing science product accuracies. HOPS COTS has been built and tested using a variety of data sets. A HOPS COTS system was built with an A/D conversion capability in order to test the HOPS COTS end-to-end in real time. The science product accuracy testing was also conducted to verify the accurate functionality of HOPS COTS.

The HOPS team plans to participate in a flight demonstration with a project ACES (ASCENDS CarbonHawk Experiment Simulator) with the current HOPS COTS system. ACES is an ESTO Instrument Incubator Program (IIP) project and its goal is to advance technologies critical to measuring atmospheric column CO₂ mixing ratios in support of ASCENDS. The platform will be either the NASA's flight laboratory DC-8 based at NASA Dryden Flight Research Center (DFRC) or a Hu-25 based at LaRC. ACES will provide two channels of science data and the HOPS COTS system will be put to a test processing data in real-time. The expected input data rate of ACES is 4 million samples per second (MSPS) with 32-bit single-precision per sample. Currently, the HOPS COTS can handle higher input data rate than 4 MSPS.



Figure 5 The HOPS COTS system. It consists of an FPGA Board (HOPS COTS), an Adlink Technology Intel Core i7 system board, a 4-Channel, 14-bit, 50 MSPS A/D board, and three 250W power supplies.

The system board is responsible for transferring science data to the HOPS COTS board and reading the science products from it. The science data can be pre-recorded and stored on the hard drive for a real-time simulation. It can also be streamed from the data acquisition board that is driven by an external signal source such as a function generator.

6. CONCLUSION

HOPS is an enabler for science missions by offering a high data processing rate in real-time via high memory and inter-board bandwidths. HOPS is scalable and reconfigurable by means of a modular board concept and FPGAs. HOPS is highly adaptable to new algorithms with a short turn-around time thanks to the reusable computation elements and plug-and-play computing architecture. HOPS is unique such that the subcomponents or the computation elements of HOPS

and FPGA IP Cores are reusable, which will minimize the development time for a different application and algorithm. The adaptation to a different application and algorithm will be far easier than starting from scratch. Users don't need to understand the details of the IP.

The demonstration of ASCENDS algorithm on HOPS COTS has been completed successfully. The relative error which is defined as the absolute value of (correlation method results – FFT core results) divided by the correlation method results was in the order of 1E-6 as required by ASCENDS. The golden reference results were generated by the ASCENDS algorithm implemented in LabVIEW in double precision. The 200,000-sample-long ASCENDS data were down-sampled to 64K-long (65,536 samples) while maintaining the scientific implication of the original data. The resulting 64K-long ASCENDS test data were processed on the HOPS COTS system. Another set of test data from 3D Winds was run on the HOPS COTS for accuracy tests. The IP-core for 3-D Winds has been completed. Its demonstration on HOPS COTS is in progress. The final HOPS custom board is currently under development.

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BIBLIOGRAPHY

- [1] NRC, *Earth Science and Applications from Space: National Imperatives for the Next Decade and Beyond*, The National Academies Press, Washington, D.C., 2007.
- [2] ASCENDS, NASA Science Definition and Planning Workshop Report, NASA ASCENDS Workshop, University of Michigan, Ann Arbor, MI, 23-25 July 2008, Available at <http://cce.nasa.gov/ascends/docs.htm>
- [3] Browell, E. V., et al., "First Airborne Laser Remote Measurements of Atmospheric CO₂ for Future Active Sensing of CO₂ from Space," *Proceedings of the 8th International Carbon Dioxide Conference*, Jena, Germany, September 13-18, 2009
- [4] Browell, E. V., M. E. Dobbs, J. Dobler, S. Kooi, Y. Choi, F. W. Harrison, B. Moore III, and T. S. Zaccheo (2009b), "First airborne laser remote measurements of atmospheric CO₂ for future active sensing of CO₂ from space," *Proceedings of the 8th International Carbon Dioxide Conference*, Jena, Germany, 13-18 September. (Extended abstract and slides from presentation provided on request.)
- [5] Browell, E. V., M. E. Dobbs, J. Dobler, S. Kooi, Y. Choi, F. W. Harrison, B. Moore III, and T. S. Zaccheo (2009a), "First airborne Laser Remote Measurements of Atmospheric Carbon Dioxide," Presented at Fourth Symposium on Lidar Atmospheric Applications, 2009 AMS Annual Meeting, Phoenix, Arizona, 10-15 January. (Abstract and Video Presentation available via: http://ams.confex.com/ams/89annual/techprogram/paper_146526.htm)
- [6] Pruitt et al., (2003), "High-speed CW lidar retrieval using spectral lock-in algorithm," *Proceeding of the SPIE*, vol. 5154, p 138
- [7] Dobbs, M., Pruitt, J., Gregory, D., & Sharp, W. 2006, "Matched Filter Enhanced Fiber-based Lidar for Earth, Weather and Exploration," AGU Fall Meeting, A1194
- [8] Active Remote Sensing using a Spectral Lock-in Technique, US Patent 6.949.734 B2
- [9] Active Remote Sensing Using a Simultaneous Spectral Sampling Technique, US Patent 7,009, 170 B2
- [10] P. Sundararajan, "High Performance Computing Using FPGAs." Xilinx WP375, Sept., 2010
- [11] T. Ng, C. Mills, "A. Bulyshev, and R. Hodson, Lidar Image Processing Acceleration Via FPGA Implementation" (abstract, presentation). In ReSpace/MAPLD Conference, 2010

- [12] R. Hodson, K. Somervill, J. Williams, N. Bergman, R. Jones III, "An Architecture for Reconfigurable Computing." In MAPLD Conference, 2005
- [13] Petrick, D, "SpaceCube: Current Missions and Ongoing Platform Advancements." In MAPLD Conference, 2009.
- [14] "Aitech S950 Single Board Computer," In <http://www.rugged.com/s950.htm#>