



# Single-Event Effect Response of a Commercial ReRAM

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# Acronyms

- **SEE – Single-event effect**
- **SEU – Single-event upset**
- **SEFI – Single-event functional interrupt**
- **RAM – Random access memory**
- **ROM – Read-only memory**
- **ReRAM – Reduction-oxidation random access memory**
- **1T1R – 1 transistor 1 resistor**
- **LET – Linear energy transfer**
- **CMOS – Complimentary metal-oxide-semiconductor**



# Motivation

- **Limited availability of radiation tolerant flash memories**
- **Radiation performance of state-of-the-art flash is generally good but include some weaknesses**
- **Flash already reaching scaling limits**
- **Resistive random access memory has shown very good tolerance to ionizing radiation\***
- **Currently available radiation test results only on test chips**
- **A first look at the SEE performance of a commercial production-level reduction-oxidation random access memory (ReRAM)**

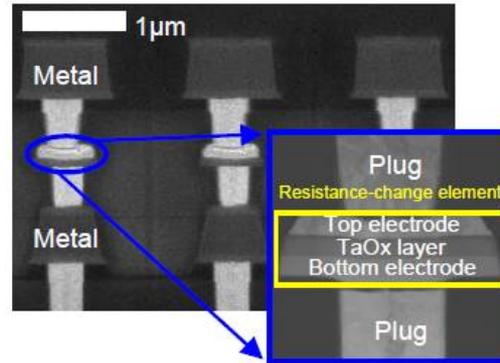
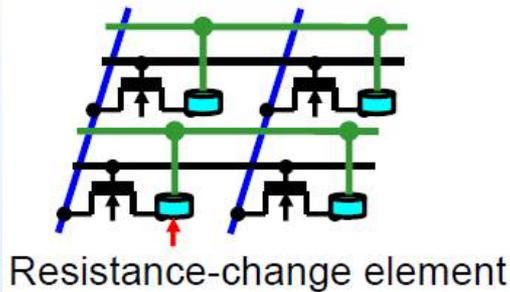
\* M. J. Marinella, S. M. Dalton, P. R. Mickel, P. E. Dodd, M. R. Shaneyfelt, E. Bielejec, G. Vizkelethy, and P. G. Kotula, "Initial assessment of the effects of radiation on the electrical characteristics of TaO<sub>x</sub> memristive memories," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 2987 – 2994, Dec. 2012

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J. S. Bi, Z. S. Han, E. X. Zhang, M. W. McCurdy, R. A. Reed, R. D. Schrimpf, D. M. Fleetwood, M. L. Alles, R. A. Weller, D. Linten, M. Jurczak, and A. Fantini, "The Impact of X-Ray and Proton Irradiation on HfO<sub>2</sub>/Hf-Based Bipolar Resistive Memories," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 4540 – 4546, Dec. 2013.

# Device Details

## 1T1R-ReRAM Memory Cell

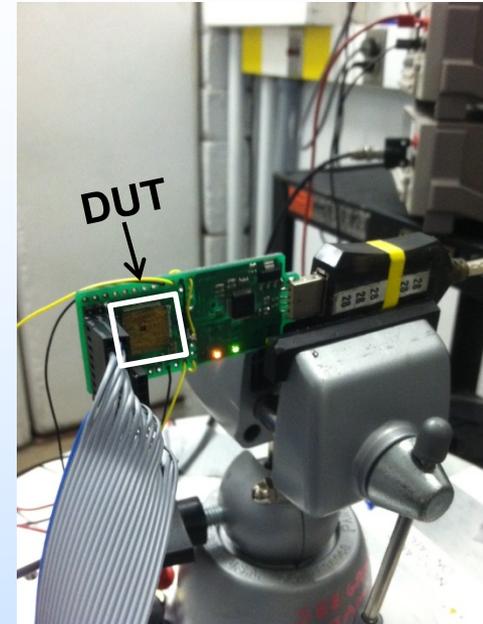
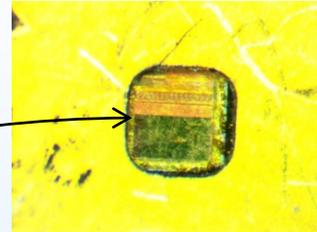
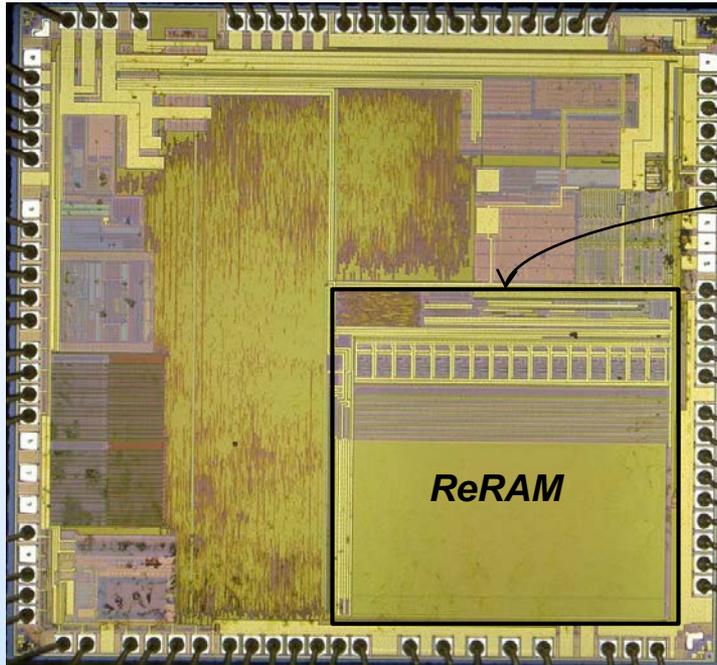


- **Panasonic MN101L**
  - 16 bit microcontroller with embedded ReRAM
  - Industry's first mass production-level ReRAM
- **1T1R array architecture, with CMOS transistor as access transistor to each ReRAM stack**
- **TaO<sub>x</sub> as switching layer**
- **Minimum device width ~ 0.5 μm**
- **Fabricated back-end-of-line in a 180 nm CMOS process**

Function	Description
Memory Size	64 KB
Program Endurance	Program area (62 KB): $\geq 10^3$ Data area (2 KB): $\geq 10^5$
Programming Voltage	1.8 to 3.6 V
Reading Voltage	1.1 to 3.6 V
Data Retention	10 years

<http://www.semicon.panasonic.co.jp/en/products/microcomputers/mn101l>

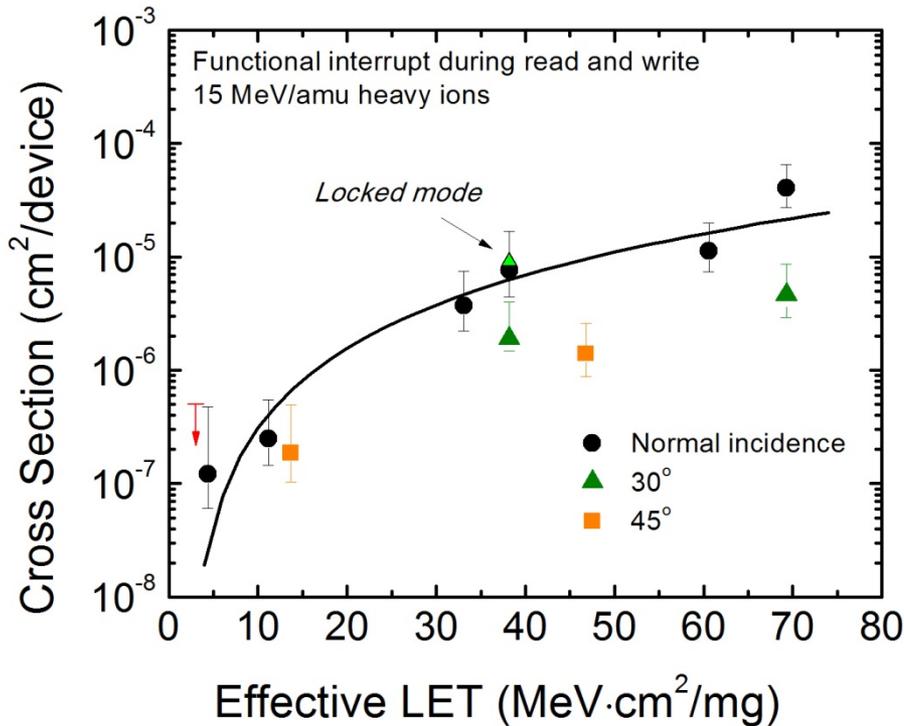
# Heavy Ion Testing



Microphotograph courtesy of JPL

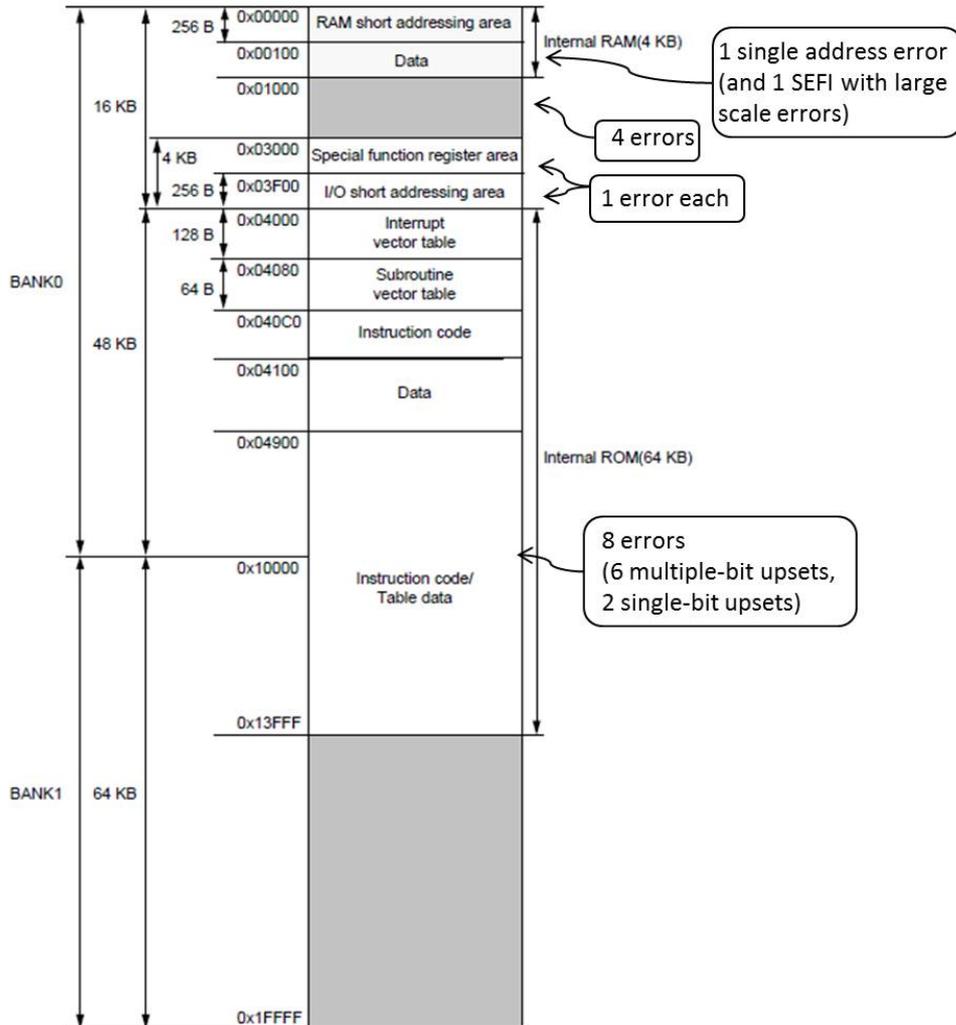
- Kovar lid collimator (254  $\mu\text{m}$ ) exposed ReRAM array and peripheral control circuits
- Used Panasonic's evaluation card as test vehicle
- Read Only Memory (ROM) operating conditions:  $V_{\text{CC}} = 3.3 \text{ V}$ , Frequency = 8 MHz or DC
- Test modes: static, dynamic read, read/compare/write, and write
- Data patterns: 00, FF, 55, and AA
- 15 MeV/amu heavy ions at Texas A&M University
  - Ne, Ar, Kr, and Xe at normal, 30°, and 45°
  - Flux =  $10^3$  to  $10^4 \text{ cm}^{-2}\cdot\text{s}^{-1}$ , fluence =  $2 \times 10^6 \text{ cm}^{-2}$  per shot

# Heavy Ion Test Results



- **Static tests did not result in SEU**
  - 1 functional error following Xe irradiation, during read-back, recovered by a reset
- **Dynamic read and write tests resulted in mostly SEFI**
  - 1 event set device into locked mode
  - Reset for read mode SEFI
  - Reset or power cycle for write mode SEFI
- **Similar SEFI cross sections for read and write test mode**
- **Angular irradiation**
  - Cross section of normal incident degraded beam several factors higher than angular irradiation with same effective LET
  - Beam shadowing from the collimator

# SEE Characteristics



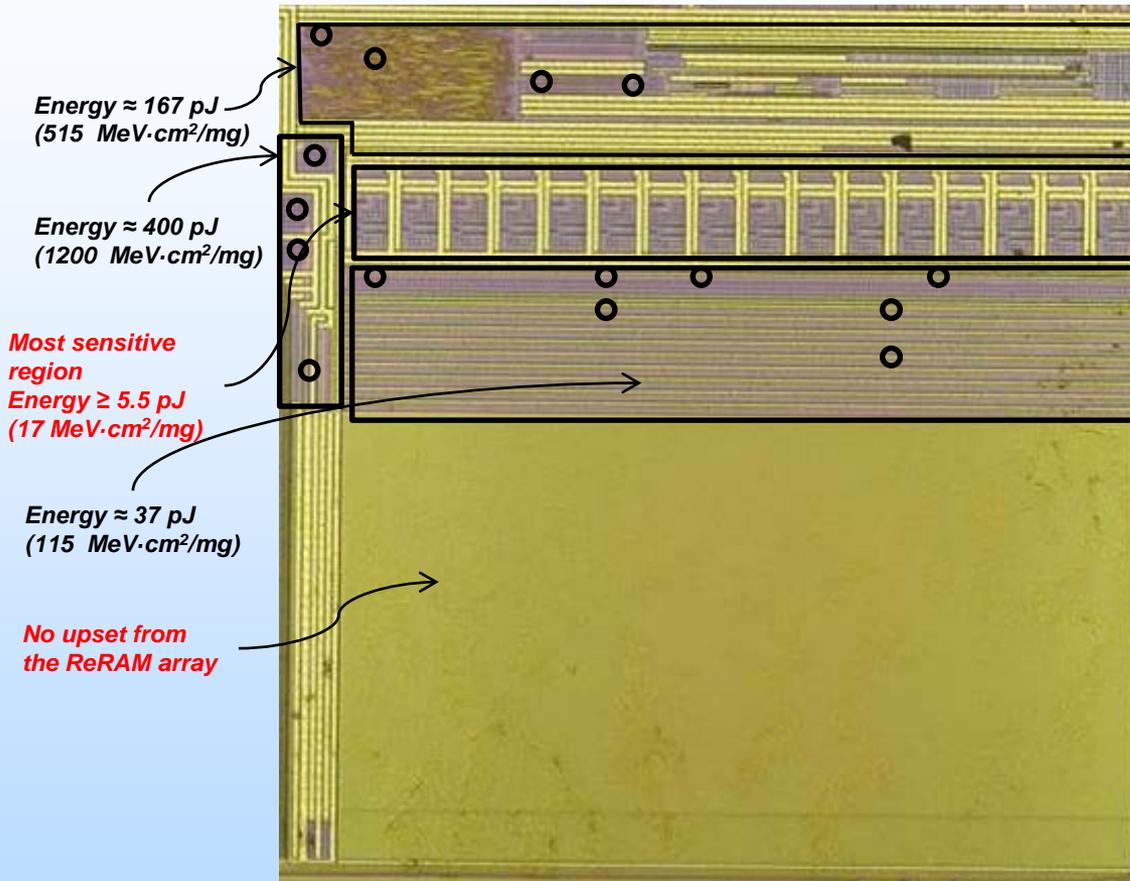
- **Functional interrupts**
  - Most SEFIs did not result in large scale errors
  - Microcontroller stops reading/writing
  - 1 SEFI showed mass errors from the RAM
- **Bit upsets**
  - Included single-bit and multiple-bit upsets
  - Error address locations distributed throughout the microcontroller memory bank
  - 8 SEUs in the ROM
  - Could not rule out array errors



# Pulsed-Laser Testing

- **Pulsed-laser testing was carried out at the Naval Research Laboratory**
- **Laser characteristics**
  - Wavelength = 590 nm
  - 1/e penetration range = 2  $\mu\text{m}$  in silicon
  - Beam diameter = 1.7  $\mu\text{m}$  for 20 $\times$  lens, 0.9  $\mu\text{m}$  for 100 $\times$  lens
- **We probed the ReRAM array and surrounding peripheral circuits with a 20 $\times$  lens to identify the sensitive regions**
- **Sensitive areas were further investigated with a 100 $\times$  lens, and the energy was fine-tuned to determine the upset energy threshold**
- **Equivalent LET values are based on empirical data from previous studies on other device types**

# Sensitive Locations



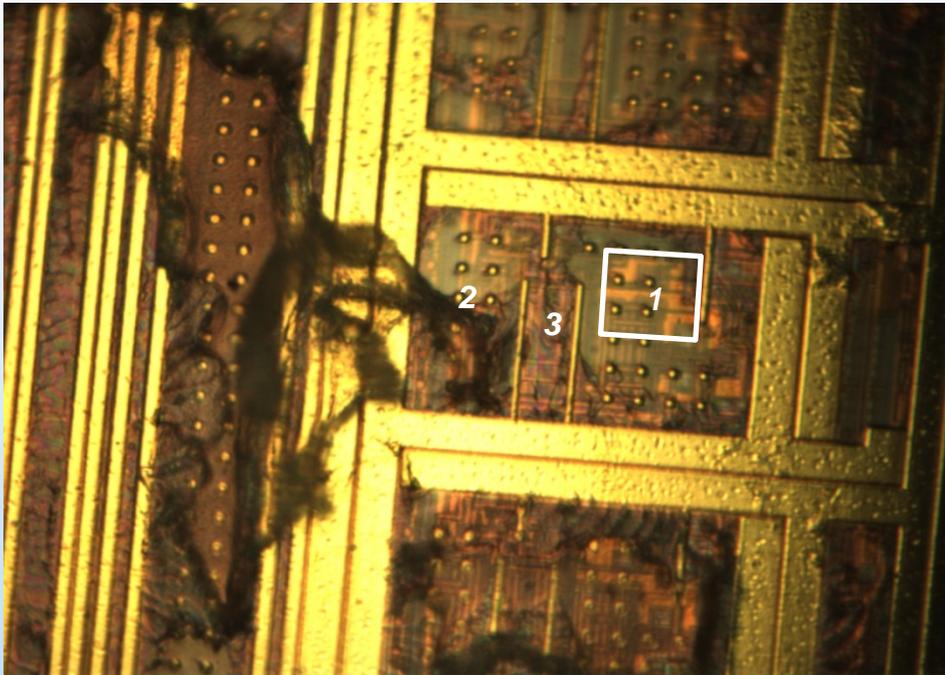
- **Bit upsets**

- Did not originate from the ReRAM array
- Location sensitive to SEUs also susceptible to SEFIs

- **Functional interrupt**

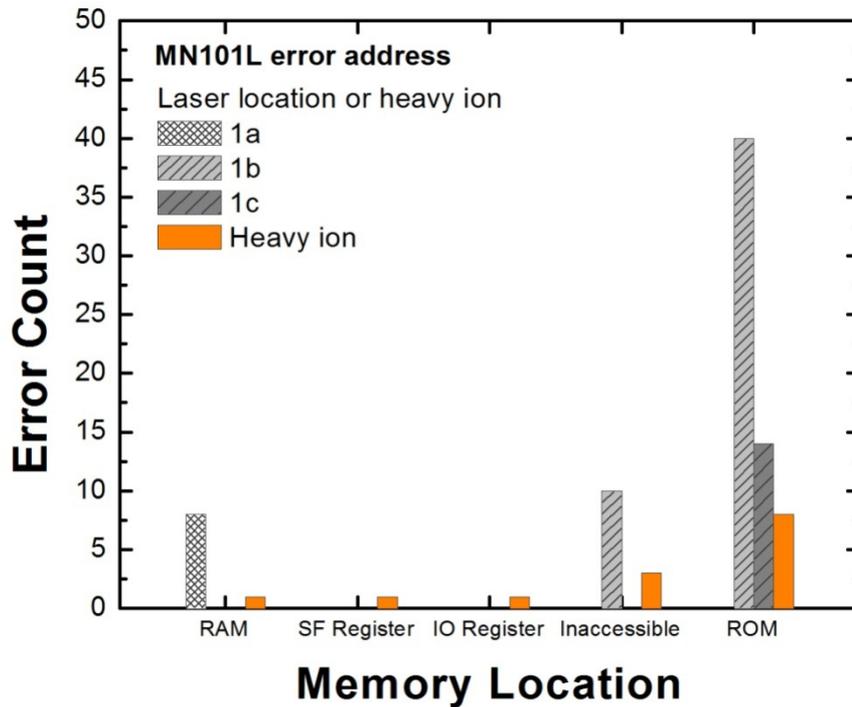
- Stops reading/writing
- Continuously reading out errors from the ROM
- Stuck reading at end of Bank0 (FFFF)
- Continuously reading errors from other address locations beside the ROM

# Upset Sensitivity in the Most Sensitive Location



- **SEFI energy threshold**
- **Location 1:**
  - Read mode: 5.5 pJ (17 MeV·cm<sup>2</sup>/mg)
  - Write mode: 8.6 pJ (26.5 MeV·cm<sup>2</sup>/mg)
- **Location 2:**
  - Read mode: 71 pJ (220 MeV·cm<sup>2</sup>/mg)
- **Location 3:**
  - Read mode: 105 pJ (320 MeV·cm<sup>2</sup>/mg)

# SEE Characteristics



- Compare SEE from location 1 with heavy ion results
- Memory address of errors from laser test are similar to those from heavy ion test
- SEFI modes from laser and heavy ion test are also similar
  - Although limited information was gained from SEFIs that caused immediate cease of operation
- Sensitive region consists of sense amplifier circuit
  - Similar characteristics to SEFI caused by SEU from sensing circuit in flash\*

SF Register – Special function register  
IO Register – Input/Output register

\* D. Nguyen and L. Scheick, "SEE and TID of emerging non-volatile memories," in Proc. IEEE Radiation Effects Data Workshop, 2002, pp. 62–66.



# Conclusion

- **ReRAM array is hardened against heavy ions with LET as high as 70 MeV·cm<sup>2</sup>/mg**
  - SEU in CMOS access transistor not enough to cause bit flip
- **SEFI is the dominant error mode**
  - Sensitivity of peripheral circuits critical to SEE response of ReRAM
  - Sense amplifier vulnerable to upsets leading to SEFI
- **Lack of charge pump reduces sensitivity to radiation-induced erase/program failure**
  - Eliminates block erase failures (issue for flash)