

Accelerated Aging Experiments for Capacitor Health Monitoring and Prognostics

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Abstract—This paper discusses experimental setups for health monitoring and prognostics of electrolytic capacitors under nominal operation and accelerated aging conditions. Electrolytic capacitors have higher failure rates than other components in electronic systems like power drives, power converters etc. Our current work focuses on developing first-principles-based degradation models for electrolytic capacitors under varying electrical and thermal stress conditions. Prognostics and health management for electronic systems aims to predict the onset of faults, study causes for system degradation, and accurately compute remaining useful life. Accelerated life test methods are often used in prognostics research as a way to model multiple causes and assess the effects of the degradation process through time. It also allows for the identification and study of different failure mechanisms and their relationships under different operating conditions. Experiments are designed for aging of the capacitors such that the degradation pattern induced by the aging can be monitored and analyzed. Experimental setups and data collection methods are presented to demonstrate this approach.

I. INTRODUCTION

Most devices and systems today contain embedded electronic modules for monitoring, control and enhanced functionality. However, it has been found that these modules are often the first elements in the system to fail thus reducing overall system reliability. Electrolytic capacitors and metal oxide semiconductor field effect transistor (MOSFET) switches are known to have the highest degradation and failure rates among all of the components [1]. DC-DC power converters are an important part of critical avionic systems. Degraded capacitors affect the performance and efficiency of the DC-DC converters in a significant manner and also impose a risk on instantiating cascading failures on other connected subsystems, such as Global positioning system (GPS) receiver, Inertial measurement unit (IMU) and software (GPS software, INAV - integrated navigation solution) components [2].

This drives the need for Integrated Vehicle Health Management (IVHM) technologies for safety critical applications, such as avionics systems. Studying and analyzing the performance degradation of embedded electronics is absolutely necessary to increase system reliability, increase system performance, and reduce maintenance costs, [3]. In addition,

an understanding of the behavior of deteriorated components is needed to anticipate failures and predict the RUL of the electronic systems.

Our focus in this work is on discussing the experimental setups to study and observe electrolytic capacitor degradation under different operating conditions. The devices are monitored closely during the degradation phase to observe and study the underlying phenomenon, which are then matched against physics based degradation models. We discuss experimental setup for nominal degradation, where the capacitors are not overstressed but operated under nominal conditions within its operating limits. But this takes longer time for the devices to degrade and studying this sometimes becomes difficult. Accelerated life test methods are often used in prognostics research as a way to assess the effects of the degradation process through time. It also allows for the identification and study of different failure mechanisms and their relationships with different observable signals and parameters. In this work we discuss the accelerated aging setups for electrical and thermal stress conditions.

The structure of the paper is as follows. Section II presents introduction to electrolytic capacitors and its basic structure, operation and degradation mechanisms. Section III discusses the nominal degradation experiments with data analysis. Section IV and V describes the experimental setups for electrical and thermal stress respectively along with data analysis. The paper ends with discussion and conclusion in section VI.

II. ELECTROLYTIC CAPACITORS

Figure (1) shows a detailed view of the cross section of an electrolytic capacitor structure. To get higher capacitance values for the same surface area of the anode and cathode foils, the foil is etched by a chemical process. Together with magnified effective surface area attained by etching the foil, a high capacitance value is obtained in a small volume [4]. In this work, we analyze non-solid aluminum electrolytic capacitors in which the electrolytic paper is impregnated with liquid electrolyte. After etching, the plates are anodized by coating them with a thin aluminum oxide layer on the surface of the foil. This layer of aluminum oxide acts as the dielectric

(insulator) and serves to block the flow of direct current between the two capacitor plates [5], [4].

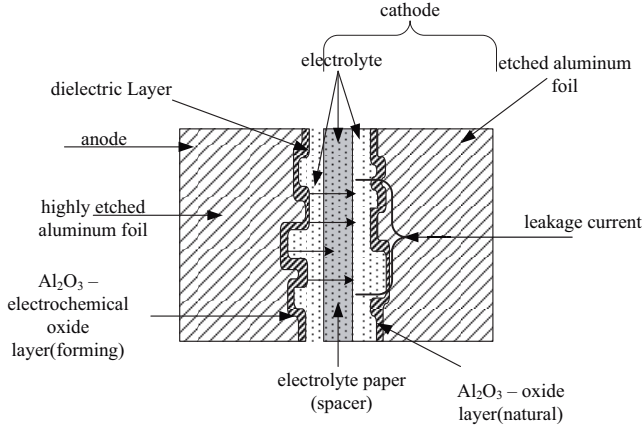


Fig. 1. Capacitor Detail Structure

Operating conditions, such as voltage, current, frequency, and ambient temperatures can have significant effects on electrolytic capacitor performance and useful life. A primary reason for degradation in aluminum electrolytic capacitors is due to vaporization of electrolyte and degradation of electrolyte efficiency due to ion exchange during the charge/discharge cycles, which in turn leads to a drift in the two main electrical parameters of the capacitor: (1) the equivalent series resistance (ESR), and (2) the capacitance. The fishbone diagram in Fig. (2) summarizes the most common set of failure modes for electrolytic capacitors that have been discussed in [6]. This diagram identifies the relationship between root causes and failure modes observed in electrolytic capacitors. These root causes can occur individually or simultaneously depending upon the conditions of operation of the capacitor.

The ESR of a capacitor is the sum of the resistances due to aluminum oxide, electrolyte, spacer, and electrodes (foil, tabbing, leads, and ohmic contacts) [5] and capacitance is the ability of a capacitor to store charge in an electric field. The health of a capacitor is often measured by the values of these two parameters. As per the industry standards [7], [8], under nominal operating conditions, capacitors are considered completely degraded and not usable in the circuit when its ESR value reaches 2.8 times of the initial ESR value and capacitance decrease in excess of 20% of the initial value.

A simplified electrical lumped parameter model of impedance, \mathcal{M}_1 , defined for an electrolytic capacitor is shown in Fig. (3). The ESR dissipates some of the stored energy in the capacitor. An ideal capacitor would offer no resistance to the flow of current at its leads.

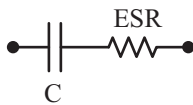


Fig. 3. Lumped Parameter Model (\mathcal{M}_1)

III. NOMINAL DEGRADATION EXPERIMENT

For this experiment, DC-DC converters having a rated input voltage of 22V-28V DC, sourced through a power supply operating at room temperature, with a constant output of 5V with ripples within the accepted noise tolerance of 1% were used. This source is likely to be 28V DC in case of avionics systems. This converter, was purchased off the shelf (which met all the specifications for the experiment). The main hardware components include the MOSFET's, isolating transformers, pulse width modulation (PWM) controller chip and an electrolytic capacitor functioning as a filter at the output. The capacitor is subjected to stresses due to long periods of operations at a constant voltage output.

Three sets of DC-DC converter hardware units were considered for the experiment. Electrolytic capacitors of 2200 μ F capacitance value, with a maximum rated voltage of 10V, maximum current rating of 1A and maximum operating temperature of 85 $^{\circ}$ C were used for the study suggested by the manufacturers of the converters. The electrolytic capacitors under test were characterized using an the SP-150 Biologic instrument [9], which measures the impedance parameters.

A. Impedance measurement

The SP-150 Biologic SAS impedance measuring instrument uses Electrochemical Impedance spectroscopy (EIS), and finds applications in corrosion, battery, fuel cell development, sensors, and physical electrochemistry. Impedance measurements can be made in a potentiostatic mode (PEIS) or in a galvanostatic mode (GEIS). The PEIS mode is used for characterizing all the capacitors under test.

An ideal capacitor has complex impedance $Z_I = 1/sC_I$ where C_I is the ideal capacitance value. The complex impedance of model \mathcal{M}_1 is given by

$$Z = R_E + \frac{1}{sC_R} \quad (1)$$

where R_E is the equivalent series resistance (ESR) and C_R is the real capacitance (C). It should be noted that the lumped-parameter model used to estimate ESR and capacitance, is not the model to be used in the prognostics algorithm; it only allows us to estimate parameters which provide indications of the degradation process through time. PEIS mode experiments perform impedance measurements by adding a small sinusoidal voltage to a DC potential that can be set to a fixed value, or relative to the cell equilibrium potential. The equation of the working electrode versus time is:

$$E_{WE}(t) = E_{WE} + V_a \sin(2\pi ft), \quad (2)$$

where V_a is the applied potential amplitude and f the frequency.

Electrochemical impedance spectroscopy measurements are available to characterize the electrical performance of the capacitor. Figure 4 shows Nyquist plots of the impedance measurements for capacitor #1 at pristine condition and after

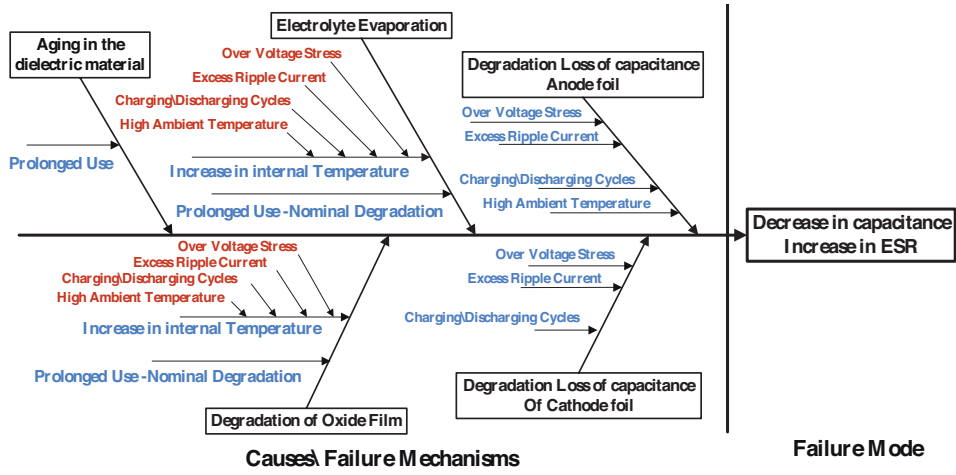


Fig. 2. Fishbone diagram of failure mechanisms in aluminum electrolytic capacitor

accelerated electrical overstress aging at intervals of 71, 161 and 194 hours. The degradation can be observed as the Nyquist plot shifts to the right as a function of aging time due to increase in R_E . These measurement are then used to estimate the parameters of the impedance model M_1 from eq. (1). The parameter estimation performed using the EIS instrument software (EC lab). This is basically an optimization problem using an aggregate of mean squared error as an objective function. The error is aggregated at different frequencies for which measurements are available. The optimization is set up to minimize the objective function by finding optimal values for C_R^* and R_E^* . This parameter estimation is performed every time an EIS measurement is taken resulting on values of C_R and R_E at different points in time through the aging of the components.

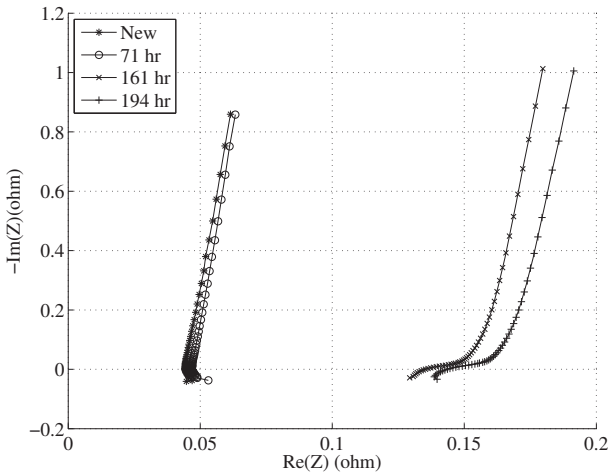


Fig. 4. Electroimpedance measurements at different aging times.

The average initial ESR value was measured to be around $49\text{m}\Omega$ and the average capacitance of $2068\mu\text{F}$ for the three electrolytic capacitors under test. The ESR measurements were made approximately every 100 hours of operations time. The

ambient temperature for the experiment was controlled and kept at 25°C . During each measurement the voltage source was shut down, all the capacitors were allowed to discharge completely before they were characterized using the impedance measurement instrument. Keeping all the conditions intact the experiment was started again till the next measurement.

B. Results

Fig. 5 shows increase in the ESR values over the period of aging for all the three capacitor units. It is observed that till 3200 hours of operation we observed almost a linear increase in the ESR value, and after 3200 hours the ESR increases at an exponential rate. At the end of 3600 hours of operation the average capacitor ESR value increased by approximately 102% of the initial value. Figure 6 shows capacitance plots for a total of 3600 hours of operation with an average decrease in capacitance (C) approximately 7.3%.

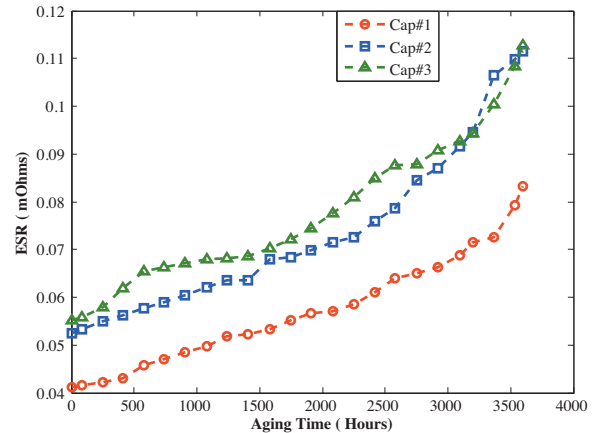


Fig. 5. Degradation in ESR parameter

A linear decrease in the capacitance is observed during the early stages of the degradation experiment and this phenomenon can be related to the decreases in the electrolyte due to a constant evaporation rate. After a certain point in

aging time a rapid decrease is observed at the knee point after 2500 hours of operation. This rapid decrease can be related to sudden breakdown in the oxide layer.

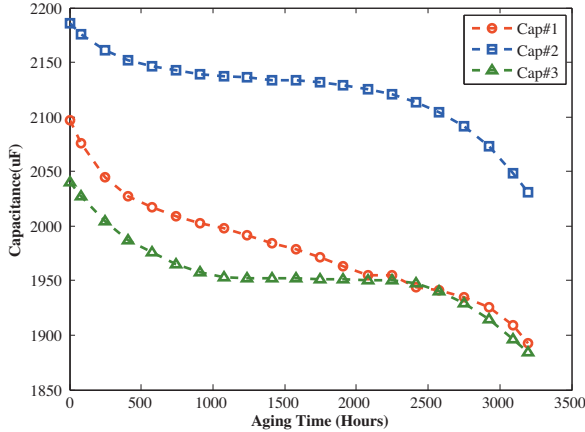


Fig. 6. Degradation in Capacitance value parameter

IV. THERMAL OVERSTRESS EXPERIMENT

In this setup we emulated conditions similar to high temperature storage conditions (no charge on capacitors) [10], where capacitors were placed in a controlled chamber and the temperature raised above their rated specification. Pristine capacitors were taken from the same lot rated for 10V and maximum storage temperature rating of 85°C. The chamber temperature was gradually increased in steps of 25°C till the pre-determined temperature limit was reached. The capacitors were allowed to settle at a set temperature for 15 min and then the next step increase was applied. This process was continued till the required temperature limit was attained. To decrease possibility of shocks due to sudden decrease in the temperature the above procedure was followed.

Experiments done with 2200 μF capacitors with TOS temperature at 105°C and humidity factor at 3.4%. At the end of specific time interval the temperature was lowered in steps of 25°C till the required room temperature was reached. Before being characterized the capacitors were kept at room temperature for 15 min. The capacitors were characterized using the EIS instrument as discussed earlier. Fig. 7 shows the plots decrease in capacitance due to accelerated aging for all the 15 capacitors under test at different aging times.

In the thermal overstress experiments, the capacitors were characterized periodically and after 3400 hours of operation it was observed that the average capacitance (C) value decreased between 9-11% while decrease in ESR value was observed around 20 - 22%. From literature [11] under thermal overstress conditons higher capaitance degradation is observed and minor degradation in ESR which correlated with the data collected. The failure thresholds under storage conditions for capacitance (C) is 10% while that for ESR is around 280- 300% of the pristene condition values [7], [8]. Hence the capacitance degradation data was used as a precursor to failure parameter to estimate the current health condition of the device.

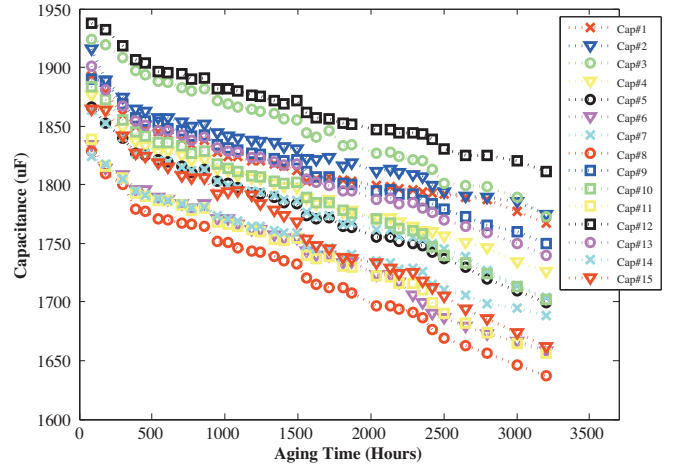


Fig. 7. Capacitance Plot for all the devices under TOS

V. ELECTRICAL OVERSTRESS EXPERIMENT

In this setup the capacitors were subjected to high voltage stress through an external supply source using a specifically developed hardware as described by block diagram in Figure 8.

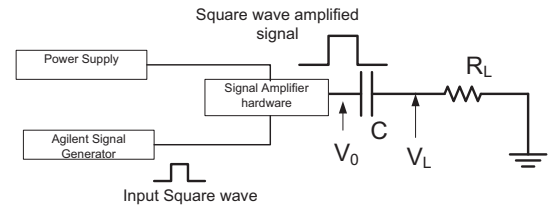


Fig. 8. Block diagram of the experimental setup.

A. Power Supply

The power supply used for the experiment is a BK Pre-cession 1761 triple output DC power supply. A constant DC voltage of $\pm 15\text{V}$ is required by the amplification hardware which is provided by this power supply.

B. Function Generator

In the experiment we are charged/discharged the capacitors at a fixed frequency using a square wave input. This input square wave was generated using a Agilent 33220A 20 MHz Function/Arbitrary Waveform Generator. This is a 14-bit, 50 MSA/s, 64 k-point arbitrary waveforms generator and can be controlled over USB, GPIB and LAN ports.

The function generator is programmed for a 1V square wave output at 100mHz. This frequency is calculated depending upon the RC time constant, where R is the load connected for the capacitor to discharge and C the capacitance values of the capacitor. At this frequency the capacitors are charged completely, stabilized at the charged value for a few seconds and then discharged completely.

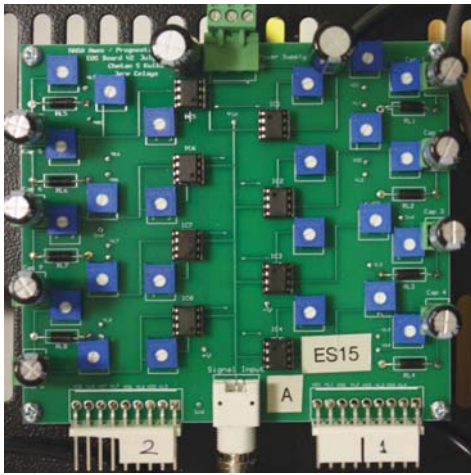


Fig. 9. Custom Module PCB developed for Signal Amplifier Hardware

C. Amplification Stage

The manufacturer rates the capacitor at maximum 10V operating voltage. To observe the degradation due to electrical charge/discharge stress on the capacitor we stress the capacitors at different voltages specifically 8V, 10V, 12V and 15V.

To generate these different voltage levels from the function generator for a same square wave input we have developed a specific hardware as shown in Fig. (9). Opamp 714 IC's are used in the inverting amplification mode with varying gains to obtain the required square wave voltages.

D. Load Resistor

To discharge the capacitor completely before the next charging cycle a resistive load was connected. The load selected is calculated such that the capacitor is completely discharged before the next charge cycle at 100mHz and the load should be able to sink sufficient amount of current to dissipate enough power. From these calculation a 1W 100Ω resistor was selected as a load.

E. Measurements

Due to the charging/ discharging cycle the internal temperature of the capacitor increases. To monitor the rise in the temperature, a temperature sensor was connected to the bare aluminum part on the top of the can. Along with this measurement we also monitored the ambient room temperature in which the experiment was conducted. The schematic shown in Fig. (8) shows the measurements taken for each capacitor.

For this experiment six capacitors of 2200μF capacitance, with a maximum rated voltage of 10V, maximum current rating of 1A and maximum operating temperature of 85°C were used for the study. The ESR and capacitance values were estimated from the capacitor impedance frequency response measured using the EIS instrument. Using the lumped parameter model, M_1 the ESR and capacitance (C) values were estimated at each measurement. The average pristine condition ESR value was measured to be 56 mΩ and average capacitance of 2123 μF individually for the set of capacitors

under test. The ambient temperature for the experiment was controlled and kept at 25°C. During each measurement the voltage source was shut down, capacitors were discharged completely and then the characterization procedure was carried out. Fig (10) shows the current EOS experimental setup, where 4 boards are running simultaneously at different voltage levels.



Fig. 10. EOS experimental setup.

Figure (11) shows percentage increase in the ESR value for all the six capacitors under test over the period of time. Similarly, Fig. (12) shows the percentage decrease in the value of the capacitance as the capacitor degrades over the aging period. During the charging/discharging process the capacitors degrade over the period of time. As described by the fishbone diagram, under EOS conditions the simultaneous underlying phenomenon of electrolyte evaporation, leakage current increase and increase in internal pressure take place.

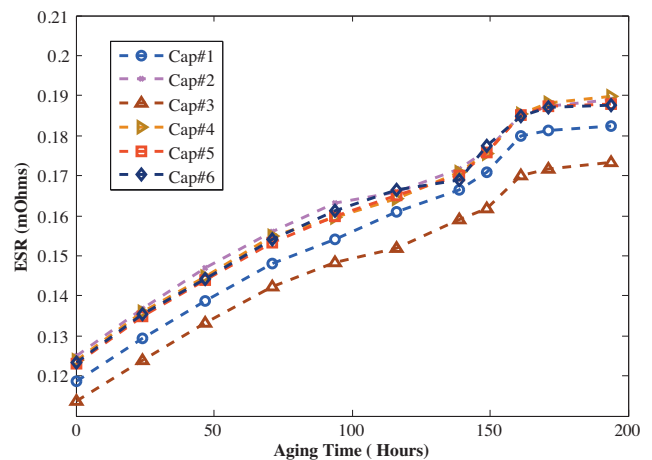


Fig. 11. Degradation of capacitor performance, percentage ESR increase as a function of aging time.

As per standards [8], a capacitor is considered unhealthy if under electrical operation its ESR increases by 280 – 300% of its initial value or the capacitance decreases by 20% below its pristine condition value. From the plots in Figure 11 we observe that for the time for which the experiments were conducted the average ESR value increased by 54% – 55% while over the same period of time, the average capacitance decreased by more than 20% (threshold mark for a healthy capacitor).

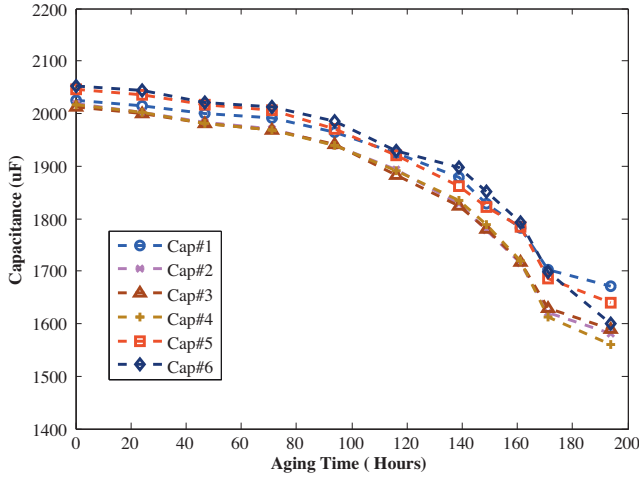


Fig. 12. Degradation of capacitor performance, percentage capacitance loss as a function of aging time.

Experiment	Capacitors	Setup	Units
Nominal Degradation	2200 μ F, 10V, 85 $^{\circ}$ C	5V, 25 $^{\circ}$ C	3
Thermal Overstress	2200 μ F, 10V, 85 $^{\circ}$ C	0V, 125 $^{\circ}$ C	8
Thermal Overstress	2200 μ F, 10V, 85 $^{\circ}$ C	0V, 105 $^{\circ}$ C	15
Thermal Overstress	10000 μ F, 10V, 85 $^{\circ}$ C	0V, 105 $^{\circ}$ C	15
Electrical Overstress	2200 μ F, 10V, 85 $^{\circ}$ C	10V, 25 $^{\circ}$ C	6
Electrical Overstress	2200 μ F, 10V, 85 $^{\circ}$ C	12V, 25 $^{\circ}$ C	8
Electrical Overstress	2200 μ F, 10V, 85 $^{\circ}$ C	15V, 25 $^{\circ}$ C	8

TABLE I
CAPACITOR DEGRADATION EXPERIMENTS : DATA SET

Table I describes the datasets for all the experiments that have been conducted to study and collect data for capacitor degradation under different operating conditions. The first column describes the type of experiment conducted, the second column in the table gives details of the capacitors used for the experiment while the third column gives the details of the experimental setup under which the capacitors were stressed. The last column indicates the number of capacitor devices used in each experiment. In the future we plan to release the data for open source for other researchers to work and implement their algorithms on capacitor prognostics.

VI. CONCLUSION

This paper presents experimental setups that have been developed for implementing prognostics methodologies for electrolytic capacitors which is the major contribution of this

work. In this work we presented separate experiments for thermal and electrical stress accelerated aging. Under actual operating conditions both these stress factors will be acting simultaneously. But working on separate experiments gave us a good idea of how the devices degrade under each of the stress conditions which in turn will help us build better and more accurate models. In our earlier work [6], [10], [12] we have implemented prognostic algorithms based on first-principles degradation model on some of the data sets and that work is still in progress.

One of the main goals that we have achieved through these experiments is to develop the capability to observe the degradation under different operating conditions. In the future work we plan to run accelerated aging experiments and by using model transformation project this data under nominal operating conditions. The data collected during the different experiments is used for estimating the different parameters and building efficient physics-based-degradation models which will enable to make better prognostics predictions. In the later stages we will be working on conducting combined stress experiments at the component level to develop degradation models as well as to study degradation effects at the system level (DC-DC converters).

ACKNOWLEDGMENT

This work was funded by the NASA Aviation Safety Program, SSAT project.

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