Assessment of SSER with respect to the ISS EPROM Memory Leakage Issue

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Purpose of presentation

- This is an informational briefing whose purpose is to
  - Review results of the assessment of the SSER with respect to the ISS EPROM Memory Leakage issue
  - Discuss an EPROM memory leakage mitigation plan for SSER, including the possibility of pre-positioning one or more spare SSERs on ISS
- This presentation has been coordinated with:
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  - EV/Bill Cowan
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EPROM Memory Leakage

- ISS Risk 6439: EPROM Memory Leakage. Regardless of whether hardware is operated or not, reprogrammable cells slowly leak off their charge which can ultimately result in loss of ORU/Subsystem functionality or failure. In many cases, there is no means of on-orbit memory refresh.
- All ISS systems' hardware containing non-volatile memory devices (e.g. EPROMs) are being assessed for this risk
- Space-to-Space Communications System (SSCS) hardware design has been reviewed by EV8 (ISS C&T System) in support of this activity

SSER Assessment

- SSER design has been reviewed in 2014 by EV8 as part of the EPROM Memory Leakage issue effort
- SSER includes three nV memory devices
  - Atmel AT28C16 EPROM
  - Simtek STK1068 nVSRAM
  - Altera EPC1213PI8 Serial EPROM (one-time-programmable)
- The Atmel and Simtek parts were originally identified by the SSER manufacturer as LL because of conservative read/write cycle and data retention specifications at worst-case temperatures, leading to an original 10 year SSER certification
- In 2008, the Atmel and Simtek parts were analyzed by NASA EEE Parts team who determined that data retention should be at least 20 years given the actual storage and operating environments, leading to a Certification extension to 2019/20 that was granted in 2009
- The Altera part was not identified as LL by Litton so was not studied
  - Now being evaluated by EEE parts (ECD end of Aug 2014)
- Plan for further Certification extension to 2024/28 has not been determined

Reprogramming the SSER

- If any of the SSER nV memory parts should ever need to be reprogrammed, this would have to be done on the ground
  - Requires ORU disassembly and reassembly (and associated retest)
  - Atmel and Simtek parts can be reprogrammed on their PCBs
  - Altera part must be replaced (one-time programmable) but is socketed on PCB
  - Programming equipment not certified for flight
- SSER manufacturer (Litton) is no longer on contract and is not available to reprogram parts
- EV SSCS lab is potentially capable of reprogramming the three nV memory parts in the SSER
  - All firmware is available
  - EV has never programmed these parts for flight SSERs
  - SSCS lab has the equipment to reprogram the Atmel and Simtek parts
  - WVS project (also EV/Bldg 44) has the equipment to reprogram the OTP Altera part
    - However, all programming equipment is dated and would need to be assessed and at least upgraded to STE or GSE class
  - Spare Altera parts are available in EV

Summary & Recommendation

- SSER design was reviewed in light of the ISS Program ISS Risk 6439: EPROM Memory Leakage opened in 2013
- The SSER contains three nV memory devices
  - Two parts are likely to have acceptable data retention behavior for the life of ISS based upon EEE Parts analysis performed in 2008 that led to certification extension to 2019/20
    - EV with FA and OD input must look at when to revisit certification for 2024/28
  - Third part is undergoing EEE Parts analysis but is expected to be a non-issue since it was not identified as LL by SSER manufacturer originally
- If it turns out to be necessary, reprogramming these devices by EV is possible if programming equipment is functional
  - funding would likely be required
- However, as mitigation against possible nV memory device failure on-orbit, ISS C&T recommends that the EVA office consider pre-positioning one or two SSERs on ISS
  - R&R procedure (2.488 EMU RADIO REMOVE AND REPLACE) exists for on-orbit change out of SSER