Enabling More than Moore: Accelerated Reliability Testing and Risk Analysis for Advanced Electronics Packaging

*Reza Ghaffarian, Ph.D., **John W. Evans, Ph.D.
Jet Propulsion Laboratory, California Institute of Technology
** NASA HQ, Office of Safety and Mission Assurance, Washington, D.C.
Tel: (818) 354-2059, Reza.Ghaffarian@JPL.NASA.gov
Tel: (202-358-0937), John.w.Evans@NASA.gov

ABSTRACT

For five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in miniaturization of electronics products—Moore's Law. Now, scaling hits a brick wall, a paradigm shift. The industry roadmaps recognized the scaling limitation and project that packaging technologies will meet further miniaturization needs or a.k.a "More than Moore". This paper presents packaging technology trends and accelerated reliability testing methods currently being practiced. Then, it presents industry status on key advanced electronic packages, factors affecting accelerated solder joint reliability of area array packages, and IPC/JEDEC/Mil specifications for characterizations of assemblies under accelerated thermal and mechanical loading.

Finally, it presents an examples demonstrating how Accelerated Testing and Analysis have been effectively employed in the development of complex spacecraft thereby reducing risk. Quantitative assessments necessarily involve the mathematics of probability and statistics. In addition, accelerated tests need to be designed which consider the desired risk posture and schedule for particular project. Such assessments relieve risks without imposing additional costs and constraints that are not value added for a particular mission. Furthermore, in the course of development of complex systems, variances and defects will inevitably present themselves and require a decision concerning their disposition, necessitating quantitative assessments. In summary, this paper presents a comprehensive view point, from technology to systems, including the benefits and impact of accelerated testing in offsetting risk.

ELECTRONICS PACKAGING TREND

As with many advancements in the Electronics Industry, consumer electronics is driving the trends for electronic packaging technologies toward reducing size and increasing functionality. In the past, there was always a ceramic version of a plastic package, including the plastic ball-grid-array (PBGA) which has the analogous ceramic ball-grid-array (and column-grid-array) (CBGA & CCGA). Today, there are few, if any, ceramic (high reliability) versions of the latest technologies. In fact, as with the BGA packages, ceramic packaging may not always be the most reliable choice when taking into account the board mounting process. Solder joint reliability has become an integral part of the Electronic Packaging equation for overall reliability [1-10].

Microelectronics are meeting the technology needs for higher performance, reduced power consumption and size, and off-the-shelf availability. Due to the breadth of work being performed in the area of microelectronics packaging, this paper presents only a few key packaging technologies detailed in three industry roadmaps for conventional microelectronics [11-13]. The three key industry roadmaps and current revisions of roadmaps are: (1) the 2012 reports of the international technology research society (ITRS), (2) the 2013 roadmap reports of the international manufacturing initiative (iNEMI), and (3) the 2013 roadmap of association connecting electronics industries (IPC). The objectives of each roadmap society are summarized in Figure 1, showing their emphasis on each stage of technological development, industry, and pull/push styles of implementation.

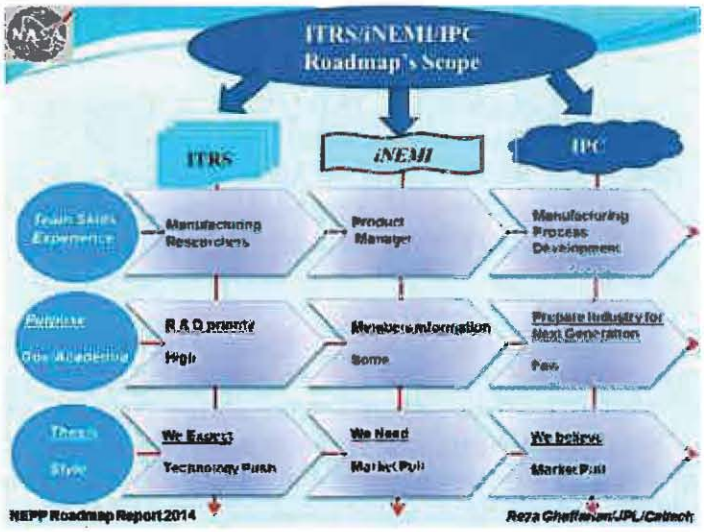

Figure 1. ITRI, iNEMi, and iPC roadmap focus and development Styles.

Moore's Law also sometimes called scaling, predicts significant trend in decreasing cost-per-function, which has led to substantial improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics. To help guide these R&D programs in scaling, the Semiconductor Industry Association (SIA) met with corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of its roadmap and to begin work toward the first ITRS, published in 1999. Since then, the ITRS has been updated in even years and fully revised in between years. The latest 2012 update is available on the ITRS website [11]. Figure 2 shows the ITRS roadmap for printed CMOS Moore's Law, and beyond which is later called "More than Moore" or its abbreviation, MtM.

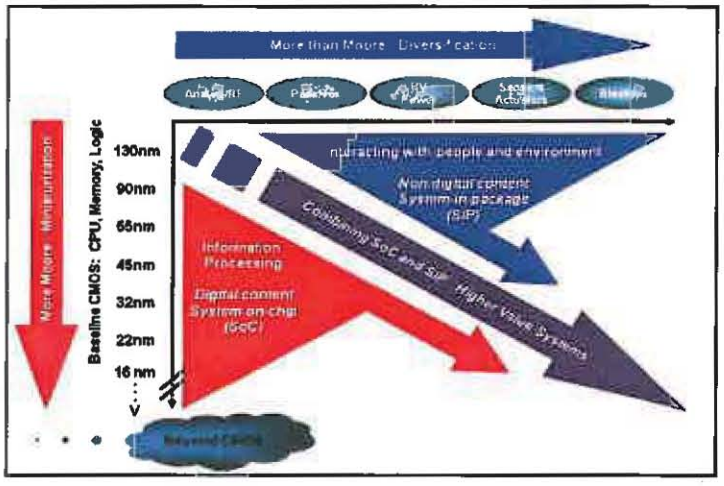

Figure 2. ITRS Roadmap for printed CMOS Moore's Law and beyond, MtM [11].

The ITRS projects that by 2020–2025, many physical dimensions are expected to be crossing the 10 nm threshold. As dimensions approach the 5–7 nm range, it will be difficult to operate any transistor structure that is utilizing CMOS physics as its basic principle of operation. It is projected that the

new devices such as tunnel transistors could provide a smooth transition from traditional CMOS to this class of devices to reach the levels of required further miniaturization. However, it is becoming clear that fundamental geometrical limits are reached in the timeframe. By fully utilizing the vertical dimension, it is possible to stack layers of transistors on top of each other. The 3D transistor approach continues to increase the number of components per mm^2 even when horizontal physical dimensions are no longer be amenable to any further reduction.

ITRS recognized the limitations of Moore's law (i.e., linear scaling) and proposed a methodology to identify those MtM technologies for which a roadmapping effort is feasible and desirable. The semiconductor community needs to depart from the traditional scaling "technology push" approach and involve new constituencies in its activities. ITRS materialized this new approach in 2011, when it added a MEMS chapter to the roadmap; it also aligned it with the iNEMI roadmap. The MEMS chapter aligns its effort towards those MEMS technologies associated with "mobile internet devices," a driving application broad enough to incorporate many existing and emerging MEMS technologies.

Single Chip Microelectronics Packaging Trend

The trend in single packaging technology is illustrated in Figure 3. Single-chip microelectronic packaging technologies are categorized into three key technologies: (1) plastic ball grid arrays (PBGAs), (2) ceramic column grid arrays (CGAs), and (3) and smaller foot prints such as quad-flat no-lead (QFN) and wafer level packages. There are numerous variation of packages in each cate-gory. Single chip packages including BGAs and chip scale packages (CSPs) are now widely used for many electronic applications including portable and telecommunication products. The BGA version has now considered for high reliability applications with generally much harsher thermal and mechanical cycling requirements than those for commercial use. Technical challenges for BGA/CSP packages include the behavior of solder joints under thermal and mechanical loading have become moving target to meet development in higher density die with associate continuously increasing in pin counts (I/Os), decreasing in pitches, and newly introduced packaging styles.

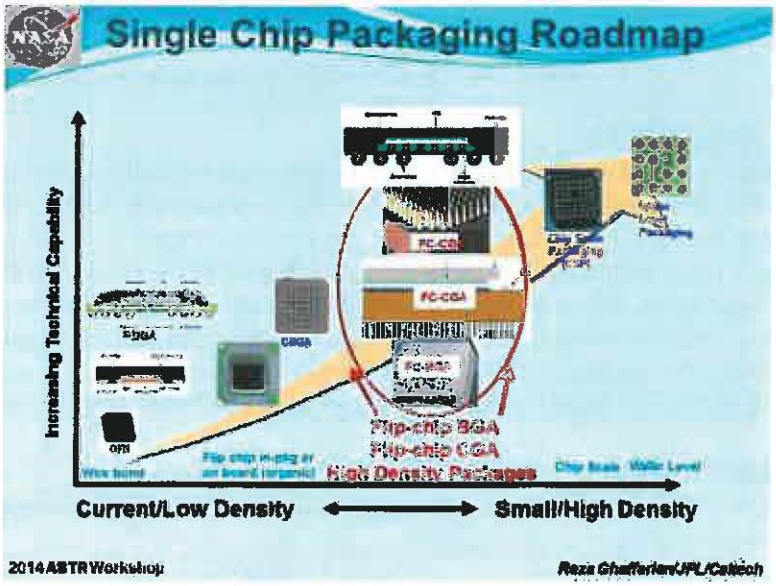

Figure 3. Microelectronic trends for single packaging technologies.

For high reliability applications, there is a continuous need to understand behavior under thermal stresses as the I/O of CGA packages increase and become more complex with using non-hermetic flip-chip die and added passives (see Figure 4). Thermal stress due to column attachment for LGA and/or reworked CGA packages affects reliability. Assembly of LGA directly onto board using con-

ductive adhesive may become a viable option in a near future possibly using adhesive with nano-particulates or other approaches. Thermal characterization of early version of high I/O PBGAs with wire bond and advanced higher I/O version with flip chip die are critical for use in harsher environmental applications.

Evaluation of CSPs including wafer level CSP (WLCSP) should be selective at this time since packaging technologies are yet to show thermal resistance robustness required for high reliability applications. With commercial industry mostly implemented Pb-free solders that added currently additional challenge for high reliability applications. The options left for use of tin-lead solders are either to continue to use tin-lead solder with Pb-free columns/solder balls (backward compatibility), replace Pb-free balls/columns with tin-lead, and accommodate Pb-free in a near future with understanding associated risks and development of mitigation approaches.

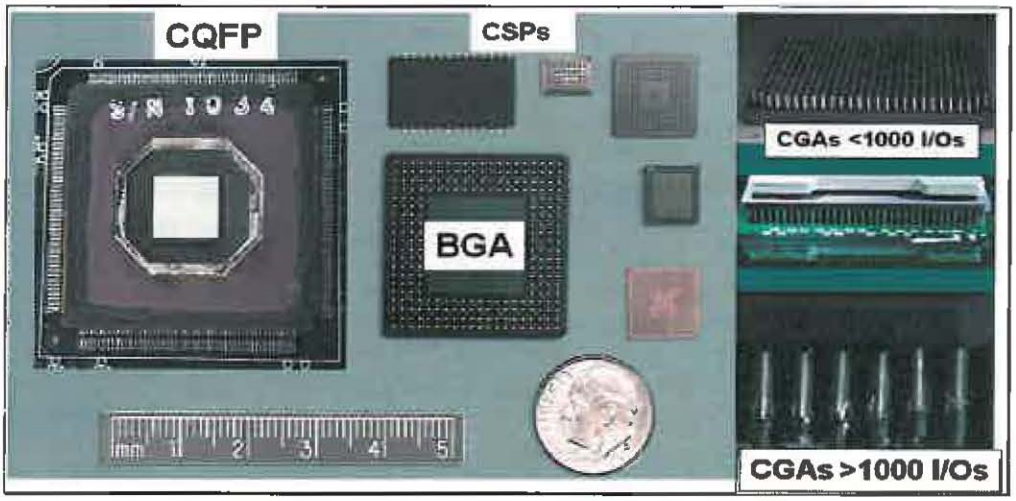

Figure 4. Surface mount (SMT) electronics packaging, from ceramic quad flat pack (CQFP) to ball grid array (BGA) and ceramic column grid array (CCGA/CGA) and chip scale package (CSP).

Ball Grid Array (BGA)

Ball grid arrays with 1.27-mm pitch (distance between adjacent ball centers) and finer pitch versions with 1- and 0.8- mm pitches, are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). Figure 5 shows schematically a typical low I/O plastic BGA with internal wire-bond and its higher I/O version with flip-chip die (FC-BGA) package configurations. BGAs provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to conventional surface mount (SMT) leaded parts. Finer pitch area array packages (FPBGA), a.k.a CSPs, are further miniaturized versions of BGAs, or smaller configurations of leaded and leadless packages with pitches generally less than 0.8 mm.

Advantages of BGAs

BGA packages offer several distinct advantages over fine-pitch surface mount components having gull wing leads, including:

- High-I/O capability (100s to approximately 3000 balls can be built and manufactured, but gull-wing leads are limited to less than 300 I/Os.)
- Higher packaging densities (This is achievable since the limit imposed by package periphery for the gull wing leads is not applicable in the case of area array packages because area rather than periphery is used; hence, it is possible to mount more packages per the same board area.)

- Faster circuitry speed than gull wing surface mount components (SMCs) because the terminations are much shorter and therefore less inductive and resistive
- Better heat dissipation because of more connections with shorter paths
- Conventional SMT manufacturing and assembly technologies such as stencil printing and package mounting

These packages are also robust in processing. This stems from their higher pitch (typically, 0.8–1.27 mm), better lead rigidity, and self-alignment characteristics during reflow processing. This latter feature, self-alignment during reflow (attachment by heat), is very beneficial and opens the process window considerably.

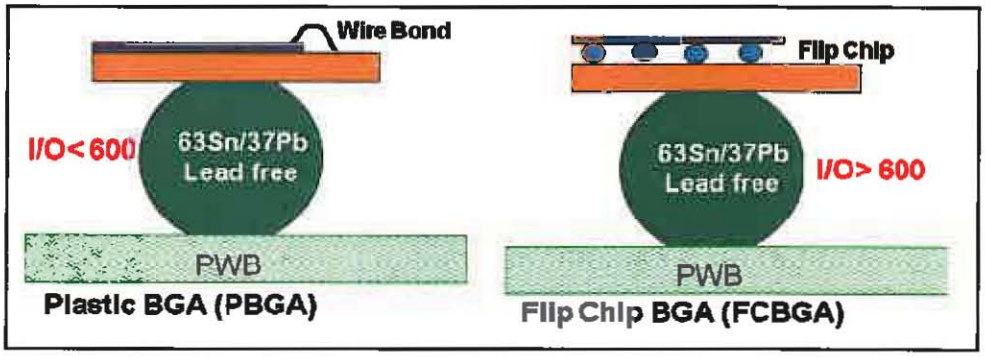

Figure 5. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

Disadvantages of BGAs

Area array packages, however, are not compatible with multiple solder processing methods, and individual solder joints cannot be inspected and reworked using conventional methods. In low volume SMT assembly applications, the ability to inspect the solder joints visually has been a standard inspection requirement and is a key factor for providing confidence in the solder joint reliability. Advanced inspection techniques, including X-ray, need development to provide such confidence for BGA and FPBGAs.

The four chief drawbacks of area array packages are:

- Lack of direct visual inspection capability
- Lack of individual solder joint re-workability
- Interconnect routing between the chip and the PWB requiring a multilayer PWB
- Reduced resistance to thermal cycling due to use of rigid balls/columns

Column Grid Array (CGA)

For high reliability applications, surface mount leaded packages, such as ceramic quad flat packs (CQFPs), are now being replaced with CGAs with a 1.27-mm pitch (distance between adjacent columnl centers) or lower. Replacement is especially appropriate for packages with higher than 300 I/O counts, where CQFP pitches become fine, making them extremely difficult to handle and assemble. In addition to size reduction, CGAs also provide improved electrical and thermal performance; however, their solder columns are prone to damage, and it is almost impossible to rework defective solder joints. Rework, re-column, and reassembly may be required to address solder defects due to processing or column damage prior to assembly due to shipping and mishandling, potentially adding cost.

CGA packages are preferred to CBGA (see Figure 6) since they show better thermal solder joint reliability than their CBGA counterparts. Superior reliability is achieved for larger packages and for higher than 300 I/Os when resistance to thermal cycling is further reduced with increasing package size. All ceramic packages with more than 1,000 I/Os generally come in the CCGA style with 1-mm pitch or lower in order to limit growth of the package size.

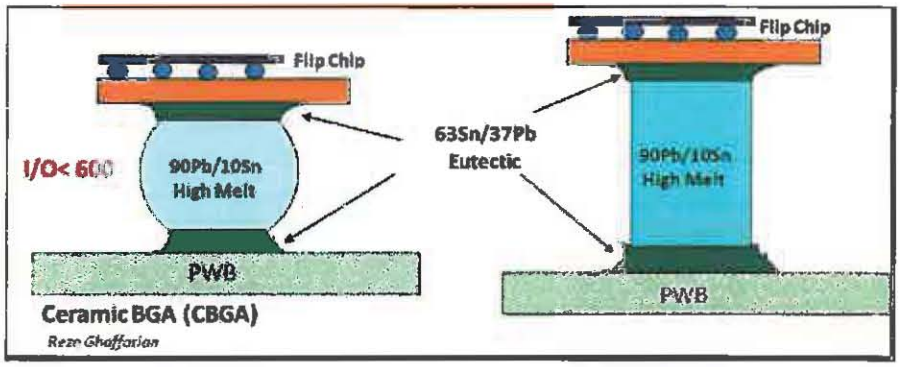

Figure 6. Examples of ceramic column grid array (CCGA) and ceramic ball grid array (CBGA) package configurations.

Key recent trends in electronic packages for high reliability applications are as follows:

- Ceramic quad flat pack (CQFP) to area array packages
- CBGA to CCGA/CGA (>500 I/Os) and land grid array (LGA)
- Wire-bond to flip-chip die within a package
- Hermetic to non-hermetic packages (>1000 I/Os)
- High-lead solder columns to columns with Cu wrap
- Pb-Sn to Pb-free, including potential use of a Cu column
- Land grid with conductive interconnects rather than Pb-free solder

The key drawback of CGAs remains the same as area array packages: individual column reworkability and inspection capability for interconnection integrity is poor (e.g., cracks and cold solder). Implementation of process controls is critical to achieving quality solder joints, which consequently achieves optimum assembly reliability. Visual inspection of peripheral columns, when they are not blocked, can be performed by optical microscopy to ensure solder quality as another process indicator. Although progress has been made in improving the resolution of X-ray for better inspection, the issue of inspection remains partially unresolved.

CGAs are often commercial-off-the-shelf (COTS) packages; their high reliability package versions go through a more stringent screening with added cost and long-time delay in delivery schedule. The issues with CGA COTS packages are essentially the same as other COTS issues and include package die source and materials variations from lot to lot, availability of packages with radiation-hard die, outgassing for materials, etc. Assembly, inspection, and lack of individual solder reworkability issues are additional key aspects of such implementation.

ACCELERATED THERMAL STRESS FOR MICROELCTRONICS SYSTEM

Reliability under thermal stress for package and assembly depends on the reliability of constituent elements and global/local interfaces (attachments) [14]. Solders in surface mount are unique since they provide both electrical interconnection and mechanical load-bearing element for attachment of package on PCB and often function as a critical heat conduit too. A solder joint in isolation is neither

reliable nor unreliable; reliability has meaning only in the context of interconnections either within package or outside of package on PCB when the PCB assembly is deployed.

Solder joints are a key interface element for BGA/CBGA/CGA package and assembly on PCB. As schematically shown in Figure 7, three elements play key roles in defining reliability for CGA, global, local, and solder alloy. In CGA, solder columns also act as load carrying element between package and boards similar to metallic leads such as those for CQFP. The characteristics of these three elements — package (e.g., die, substrate, solder joint, underfill), PCB (e.g., polymer, Cu, plated through hole, microvia), solder joints (e.g., via balls, columns) — together with the use conditions, the design life, and acceptance failure probability for the electronic assembly determine the reliability of BGA/CBGA/CGA assemblies.

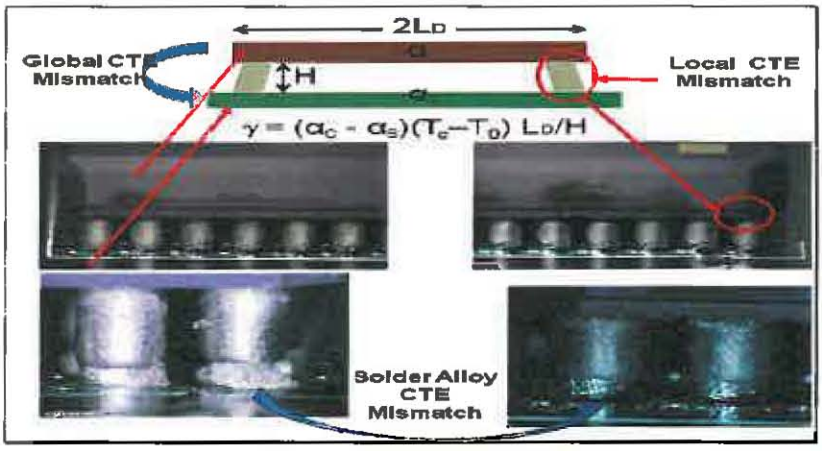

Figure 7. Three key elements defines reliability under thermal stress are due to global, local, and solder alloy coefficient of thermal (CTE) mismatches.

In other words, acceptable reliability is the ability of a system (here microelectronics) to function as expected under the anticipated operating conditions for an expected time period without exceeding the expected probability of failure. However, reliability is threatened by infant mortality due to workmanship defect and lack of sound manufacturing, and reliability design. Designs for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on, are prerequisites to assure the reliability of the product. Only a design for reliability (DfR) can assure that manufactured to quality will be reliable. The elements of the system reliability is schematically shown in Figure 8 which are comprised of device/package/PCB and interconnections and also includes consideration of design for reliability prior to assembly and subsequent manufacturing and quality assurance implementation.

Figure 8. System reliability achieved through design for reliability (DfR), sound manufacturing, and quality to packaging/device/PCB and interconnections.

Accelerated Thermal Stress for Packaging

Typical packaging build steps are schematically shown in Figure 9. After wafer processing and testing, the wafer is generally sawed into die, which are then packaged or used as chip-on-board flip chip direct attachment. In WLP, protection and testing are first performed on the wafer and then dicing in preparation for SMA. There is a great contrast between processing at the chip and package levels, including the defects created and the reliability implications involved. Materials and process steps involved may need to be modified in order to achieve reliable package for application in a harsher environment including cold or hot environment for high reliability applications.

Packaging materials and structures are chosen to meet the demands of device use in conventional environments. Thus, metals are selected according to how well they conduct current into and out of chips, and encapsulants on their ability to encase and protect the die over commercial temperature ranges. In addition to their electrical conduction function, metals are used in packaging as mechanical supports, to conduct heat away (heat sinks), and to seal the contents. Ceramics like alumina also serve as containers for chips and often the substrates for mounting semiconductor devices. Polymers are used to hermetically encase the chips and are employed in printed circuit boards for mounting the packages.

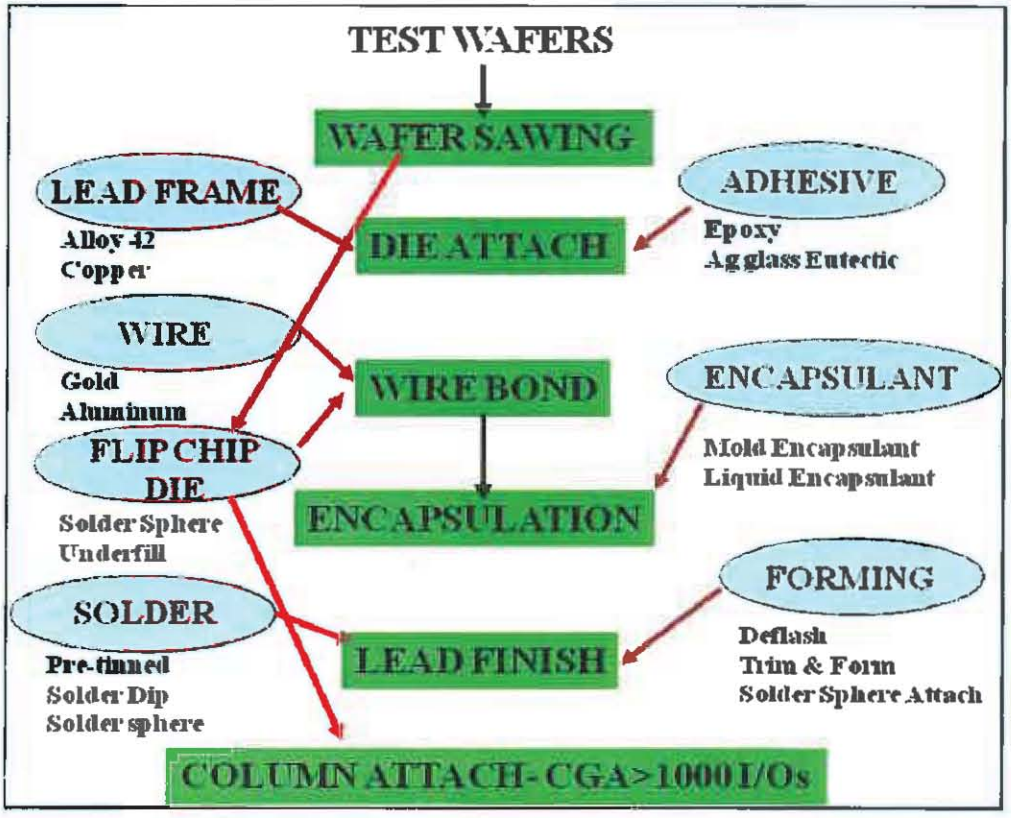

Figure 9. Microelectronic packaging steps.

Silicon of chip in package degrades under thermal stresses. Many Si device degradation mechanisms are thermally activated and the device reliability is a strong function of temperature and operating voltage. The higher the temperature, the greater are degradation mechanisms such as inter-diffusion through interconnection, latch-up, noise, and heat. For thermally activated failure mechanisms, the relative improvement in mean-time-to-failure (MTTF) with reduction in temperature is proportional to a temperature dependent term expressed by the Arrhenius relation

$$MTTF \sim \exp(E_a / K\,T) \qquad (1)$$

Where E_a is the activation energy of a given thermal process, T is absolute temperature, and K is Boltzman's constant. E_a will typically range between 0.3-1.2 eV. A lower value of E_a implies that the temperature effect is less significant for a failure mechanism than the one with higher E_a. If a value of 0.5 eV is assumed, the relative change in *MTTF* can be seen graphically in Figure 10.

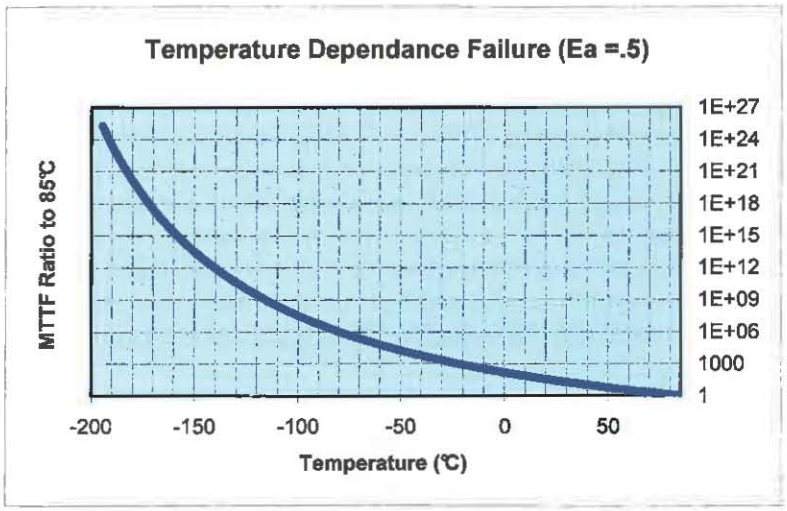

Figure 10. The effect of temperature on device MTTF when device failure has an Arrhenius relationship with E_a.= 0.5 eV

Accelerated Thermal Stress for SMT Assembly

Majority of fatigue failures of solder joints in surface mount assemblies are due to global CTE mismatch induced damage while early premature failure may be due to workmanship anomalies and local interfacial integrity deficiencies [8]. The global expansion mismatches result from differential thermal expansions of a package and the PCB assembly. These thermal expansion differences stem from differences in the coefficients of thermal expansion (CTEs) and thermal gradients as the result of heat dissipation from functional die within package. Global CTE-mismatches typically range from $\Delta\alpha$~2 ppm/°C ($2x10^{-6}$) for CTE-tailored high reliability assemblies to $\Delta\alpha$ ~14 ppm/°C for ceramic packages (e.g., CBGA/CGA) on FR-4 PCBs. The shear strain representative of the global CTE mismatch due to thermal excursion is given as the following.

$$\gamma = (\alpha_C - \alpha_S)\,(T_c - T_0)\,L/H = (\Delta\alpha)\,(\Delta T)\,L_D/H \qquad (2)$$

Global CTE mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch, i.e., the CTE-mismatch ($\Delta\alpha$), the temperature swing (ΔT), and the largest acting package length (L_D), a.k.a., distance to neutral point (DNP), can be large. In thermal cycling, this global expansion mismatch will cyclically stressed, and thus fatigue, the solder joints. The cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint in CBGA/CGA, causing permanent functional electrical failure that initially may be intermittent. The shear strain representing damage in each cycle is proportional to $\Delta\alpha$, ΔT, and L_D, and inversely proportional to the package /PCB separation height (H). For this reason CGAs are selected

for higher package sizes and I/Os since thermal strain is lower for higher column height (H) than their CBGA counterparts; therefore, it is expected to show better thermal cycling fatigue life.

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the package or PCB assembly. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions. Local CTE-mismatches typically range from $\Delta\alpha$ ~7 ppm/°C with copper to ~18 ppm/°C with ceramic. Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller in the order of tens of mils, e.g., 20 mils for a typical column diameter.

Solder alloy CTE mismatch cover microstructural changes due to solder alloy being a mixture of two or more elements. The grain structure of tin-lead solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by exposures at elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating fatigue damage. Figure 11 illustrated grain growth near cracks for a CGA assembly after two hundred thermal cycles in the range of −55°C to 100°C. For tin-lead solder, an internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of solder. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension, in the order of mils.

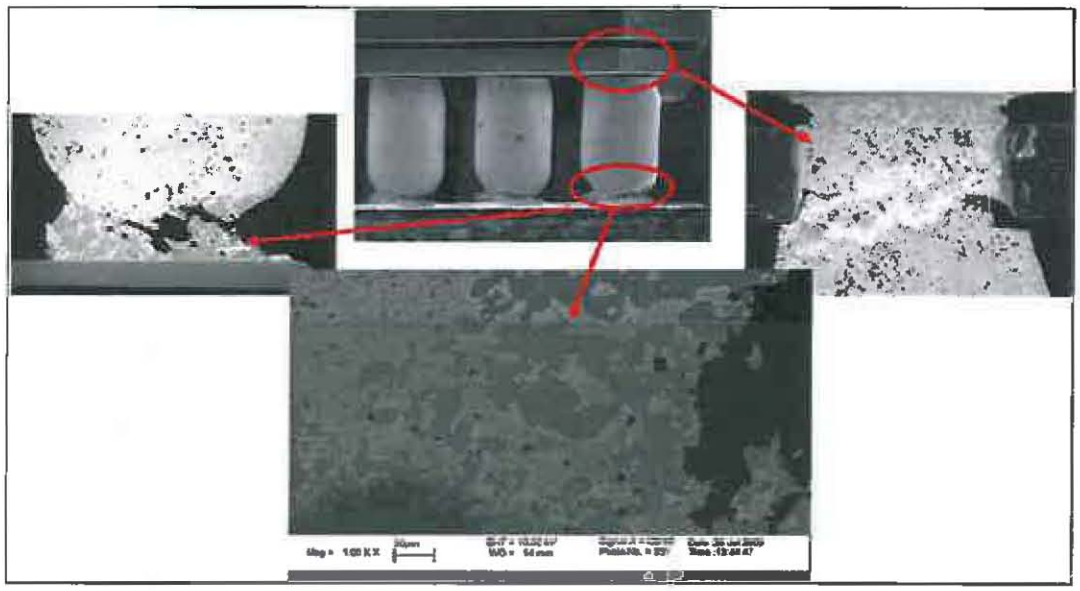

Figure 11. Tin-lead solder alloy phases and grain growth in CGA after thermal cycling.

Accelerated Thermal Cycle Fatigue Prediction Models for SMT Assembly

Predicting solder joint fatigue failure under thermal cycling stress has been one of the challenging problems for microelectronic packaging and assembly. Early solder joint fatigue models were developed based on experimental thermal cycling tests using strain gauges, therefore, mostly correlated to strains. As size of package, decreased, finite element analyses (FEA) become a more popular approach for estimating strains in PBGA/CBGA/CGA assemblies. The Coffin-Manson relationship perhaps the best known and most widely used was developed for aerospace metals and was consid-

ered for tin-lead solder. The model relates the total number of cycles to failure (CTF) to the plastic strain amplitude and the fatigue ductility coefficient and exponential.

Many fatigue models are based on modification of the Coffin-Manson relationship. One of the long-standing models used in solder fatigue analysis is the Norris and Landzberg model [24]. This relationship has been applied to project thermal cycles to failures (CTFs) for a number of conventional and advanced packaging assemblies based on accelerated test data. It is one of many numerous parametric modeling analysis methods that have been proposed and used by industry to project CTFs from one thermal cycle condition to a field application. A number of models for life extrapolation of tin-lead solder-joint attachments are listed in Table 1[7].

Table 1: Summary of various life models developed for plastic and ceramic grid array packages.

Model	Life-Prediction Representation
Coffin-Manson	$N_f = 2.277\text{x}10^{-3}(\text{Max}\ \varepsilon_{eqv})^{-2.61}$: J. H. Lau
	$N_f = 1.2938(\Delta\varepsilon_{eqv})^{-1.96}$: B. Z. Hong
	$N_f = 0.4405(\Delta\varepsilon^{eqv})^{-1.96}$: K. N. Chiang, et al.
	$N_f = K(\varepsilon_p^{-2})$: M. Farooq, et al.
	$N_f = 0.5(\Delta\gamma/2\varepsilon'_f)^{1/c}$: Howieson, M., et al
	$N_f = 82.4(De_{in})^{-0.863}$: Perkins, A., et al
Engelmaier	$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon'_f}{F}\frac{h}{L_D\Delta\alpha\Delta T_e}\right]^{-1/c}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{1/\beta}$
Norris-Landzberg	$AF = \frac{N_p}{N_t} = \left(\frac{\Delta T_t}{\Delta T_p}\right)^{1.9}\left(\frac{f_p}{f_t}\right)^{1/3} e^{1414\left(\frac{1}{T_{max,t}}-\frac{1}{T_{max,t}}\right)}$: S. Y. Teng
	$N_{50\%} = \left(\frac{100}{\Delta T}\right)^{1.9}\left(\frac{f}{2}\right)e^{1414\left(\frac{1}{T_{Max}}-\frac{1}{373}\right)}(G)$
	G=(12439-70.1A-434B-1301C-930D-272E+302CD);
	A: Substrate size, B: Board & Substrate CTE mismatch
	C: Substrate thickness, D: Board thickness, E: Ball pitch
	: A. Perkins, et al
Darveaux	$N_{init} = C_1(\Delta W_{ave})^{C_2}$; $da/dN = C_3(\Delta W_{ave})^{C_4}$
	$C_1 = 13173$, $C_2 = -1.38$ to -1.45, $C_3 = 1.72$ to 3.92, $C_4 = 1.12$ to 1.15
SRS	$N_{63.2\%} / A = C_1(\Delta W_{in})^{C_2}$ C2=-1
	: J. Clech
	$N_f = (\Delta W)^{1.51}\left(\frac{A_t}{A_D}\right)$ A_D=5.9x10-3 mm^2
	: Wong, T. E., et al

In the Coffin-Manson relationship, CTF is inversely proportional to the creep strain. Its modified version includes the effects of frequency as well as the maximum temperature. The Norris Landzberg relationship is given by:

$$(N_1/N_2) \propto (\Delta\gamma_2/\Delta\gamma_1)^{\theta} \ (f_1/f_2)^{\kappa} \exp\{(1414\ (1/T_1 - 1/T_2)\} \qquad (3)$$

N_1 and N_2 represent cycles to failure under two plastic strain conditions. θ is the fatigue exponential and is generally assumed equal to 1.9 [19, 24].

- $\Delta\gamma$ is proportional to $(DNP/h)\ \Delta\alpha\ \Delta T$, where *DNP* is the distance from the neutral point at the center of the package, *h* is equal to the solder joint height, $\Delta\alpha$ is the difference in the coefficient of thermal expansion of the package and PCB, and ΔT is the cycling temperature range, as described in equation 2.
- f_1 and f_2 are fatigue frequencies. κ is the frequency exponential varying from 0 to 1, with value 0 for no frequency effect and 1 for the maximum effect depending on the materials and testing conditions. A value equal to 1/3 is commonly used to extrapolate the laboratory accelerated thermal cycles-to-failure data with short duration (high frequency) to on/off field operating cycles with long duration (low frequency), i.e., a shorter field cycles-to-failure projection.
- T_1 and T_2 are maximum temperatures (in degrees K) under the two cycling conditions such as field and use conditions.
- The Norris-Landzberg model was developed for controlled collapse connections from thermal cycling data over a variety of temperature ranges for alloys consisting of high Pb content solder.

Acceleration factor models can be derived from any of the expressions in Table 1. It may be useful to compare more than one model in projecting accelerated data to field conditions.

ACCELERATED DYNAMIC LOADING FOR PACKAGING/SYSTEM

Mechanical methods such as shock and vibration at the package, assembly, and system levels have been an integral part of evaluation for use of microelectronics in high-reliability applications. Aerospace users have numerous specifications that address approaches on evaluating resistance to mechanical loading at various load levels for conventional packages such as leaded components. In addition, workmanship requirements to meet harsher mechanical environment are in place. For example, one of the workmanship requirement during inspection is to verify that "adhesive bonding/staking materials has been applied…for parts in excess of 7 grams (0.25 oz) per lead." Testing applicability or similar workmanship requirements are needed to be defined for advanced area array electronics both single and stack packaging technologies. Figure 12 shows an example of failure of a ceramic quad-flat package (CQFP) due to lack of sufficient mechanical support [15].

Figure 13 shows key reliability parameters under thermal and mechanical loading—creep does not play much a role in shock and vibration. The figure specifically shows details of failure mechanisms under mechanical loading for area array package and assembly. Reliability investigation of array assemblies' behavior under mechanical loading become extremely important with emergence of advanced field programmable gate arrays (FPGA) and their use in high-reliability applications. The high input/output (I/O) versions of these microelectronic devices are now come in non-hermetic underfilled flip-chip ball grid array (FCBGA) or flip-chip column grid array (CGA). Exposure of brittle die and fragile columns are two aspects that further necessitate understanding characterization of

these types of packages under mechanical loading as well as conventional thermal cycling. Since commercial industries are leading these technologies, especially those that are used in portable electronics, extensive data are available. The mechanical data generated based on industry's specifications, generally using fatigue bending and drop testing rather than under shock and vibration testing as commonly performed for high-reliability application.

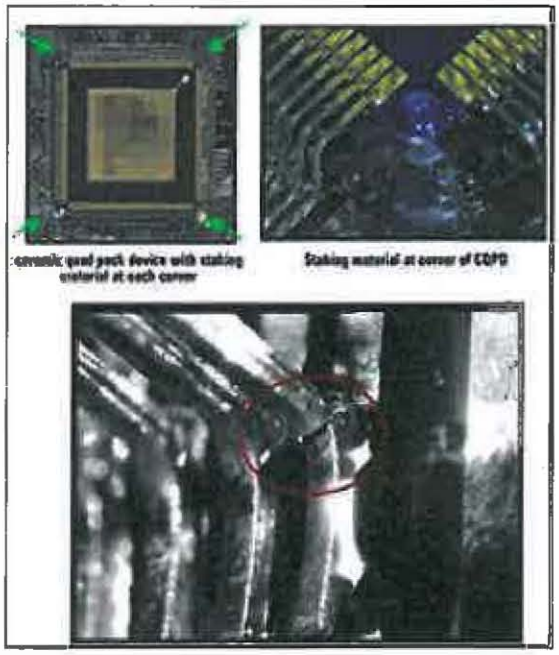

Figure 12. Lead failure for a CQFP under vibration loading due insufficient corner staking materials. (NASA Workmanship 8739.1, paragraph 4.4-3b].

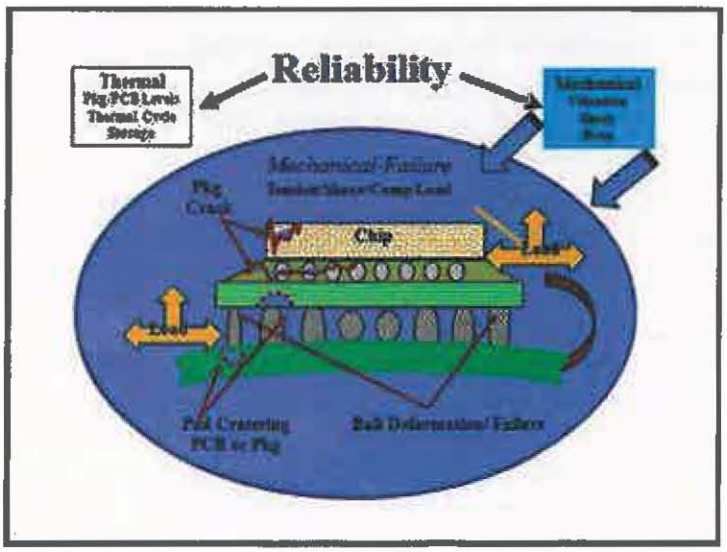

Figure 13. Thermal and mechanical reliability parameters, specifically showing failure mechanisms of advanced area array package assembly under mechanical loading including shock and vibration.

Specification on Mechanical Testing

Figure 14 lists a number of specifications generated in recent years by commercial industry particularly IPC [16] and JEDEC [17] in response to increasing demand to area array package and their miniaturized versions and stack technologies. It also include the key military specification [18] that recently in 2008 was updated.

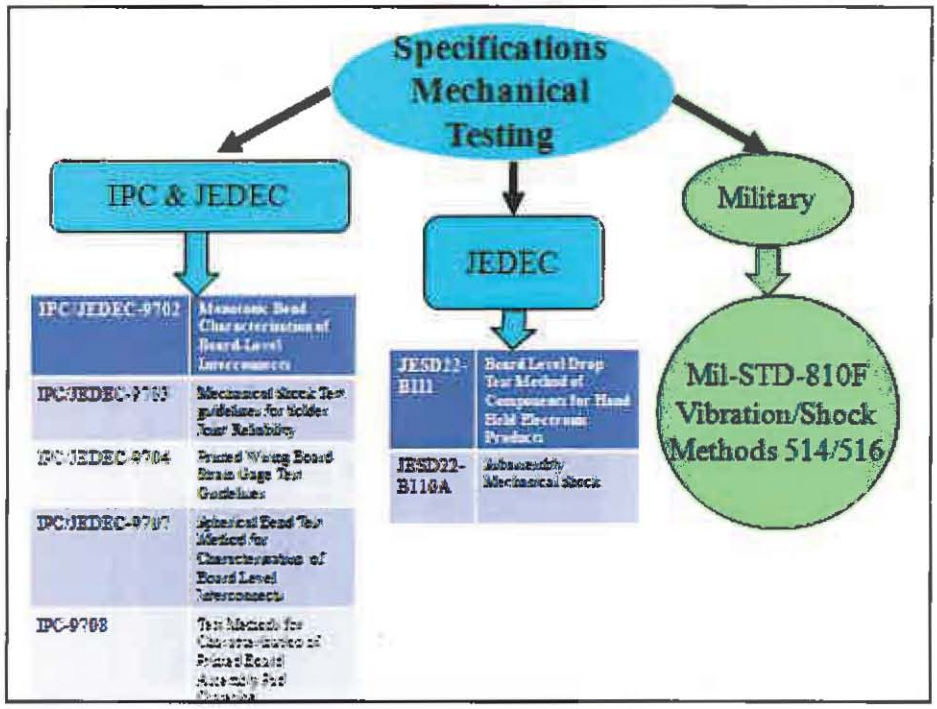

Figure 14. Key Commercial and Military specifications for mechanical testing including those for bending, drop, vibration, and shocks behavior of microelectronics and specifically advanced area array packages and 3D packaging technologies.

The key specifications that relevant to this BOK are as follows.

- IPC/JEDEC 9702 Provide cover basic mechanical bend testing characterization and strain to failure using four points bend test method commonly used also by other industry. Specific strain gage attachment delineated in IPC/JEDEC-9704.
- IPC/JEDEC 9707 covers a new test method that better applicable for area array packages, using spherical loading at points rather than loading through cylindrical as used in four point bend testing defined in 9702. The standard supplements existing standards for mechanical shock during shipping, handling, or field operation as well as fill the gap for IPC/JEDEC 9702 to better characterizes maximum strain levels. The two specifications provide a common method of establishing the fracture resistance of board-level package interconnects to flextural/point loading during PCB assembly and test operations. No pass/fail qualification requirements provided since each package/assembly considered to be unique.
- IPC 9703 cover generic guidelines for mechanical drop and shock testing since requirement for each industry is different. The scope of document includes 1) methods to define mechanical shock use-conditions, 2) methods to define system level, system board level component test board level testing that correlate to the use-conditions, and 3) guidance on the use of experimental metrologies for mechanical shock tests.

- IPC 9708 is generated in response to newly failure of board observed (pad cratering) due to move to Pb-free solder alloy implementation. Pb-free solders are generally stiffer than tin-lead solders; they can transfer more of the applied global strain to the assembly. Pb-free requires higher reflow temperatures induce higher residual stress/strains in the assembly. Pb-free typically assembled with phenolic-cured PCB materials are more brittle than conventional dicy-cured FR4 materials. These strains could eventually relax over time, but if mechanical strain is applied shortly after reflow, pad cratering could occur at lower mechanical strain levels.
- JEDEC JESD-B111 developed for portable electronics in response to need to define resistance to repeated drops required for mobile applications. Shock pulse requirement to PCB assembly is defined based on JESD22-B110 condition B Table 1 (or JESD22-B104-B Table 1) with 1500 Gs, 0.5 millisecond duration, and half-sine pulse. This specification is widely used by industry and data are of valuable for high-reliability applications. JESD-B210A defines resistance to mechanical shock.
- Mil-STD-810F covers many aspects of environmental testing including mechanical vibration and shock and is well established for conventional microelectronics for high-reliability applications.

AND RISK ANALYSIS AND MITIGATION: THERMAL CYCLING EXAMPLE

Risk Informed Systems Qualification (RISQ)

RISQ can provide a cost effective approach to maximizing the information obtained from testing system packaging designs and for qualification, as well addressing potential process variations and defects that might arise in a given assembly process. The approach for the RISQ analysis is outlined in Figure 15.

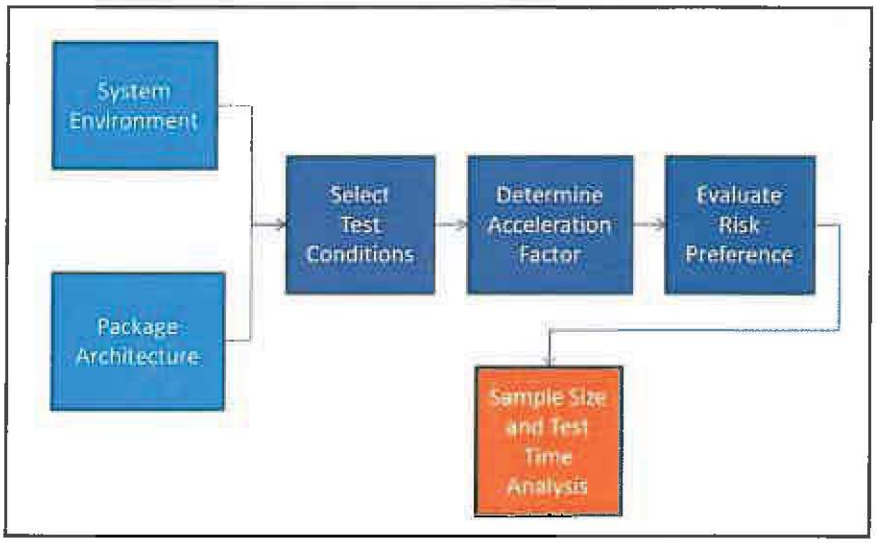

Figure 15. Risk Informed System Qualification (RISQ) Analysis process for developing accelerated testing for packaging.

RISQ can use many aspects of packaging and interconnections at different levels. As discussed in previous sections, area array packages and multiple interconnections allow effective use of the continuously improving packaging technology. As shown, there are varieties of accelerated test regimes that can be used to evaluate these packaging technologies, but these can be narrowed with consideration of the system environment. Reliable and cost effective implementation of the advanced packag-

ing schemes is needed for most systems applications, particularly for the many challenges faced in low volume and high reliability applications. High reliability applications require adequate testing and qualification strategies that can assure acceptable risks. Testing and qualification must be completed within schedule constraints to provide the necessary benefit during development.

For the space applications of microelectronics packaging systems, the environments faced by spacecraft can impose a wide range of thermal, mechanical, and shock loading on packaging and electronics assemblies. After launch, missions may serve in low earth orbit (LEO), in which a power-on and thermal cycles can occur every 90 minutes, with each orbit. Geosynchronous earth orbit (GEO), deep space, and planetary surface environments will impose a variety of thermal and mechanical challenges. The environments imposed by each of these types of missions, must be addressed in the design and then qualification, to assure mission success. RISQ method will not only maximize information obtained from the system packaging designs and qualification testing in a cost effective approach, but it also addresses potential process variations and defects that might arise in a given assembly process.

Selection of Projection Model for RISQ

System environments and selected architectures are inputs to the RISQ analysis. The environment encountered by the mission will govern the appropriate selection of test conditions and models needed to develop acceleration factors appropriate to the test design. The architectures selected are important, as materials systems and potential defect types are also important considerations in testing and test condition selection. For example, in selecting projection models for thermal cycling, a judicious evaluation of the life models shown in Table 1 is warranted. The model must be suitable to project test conditions to spaceflight use conditions for the materials and packaging configurations employed in the design.

The conditions in which an assembly will be used depend upon several design factors of the system, as well as the external environment. Under the hood automotive environment is substantially different from the cabin environment. For spacecraft, relevant system factors may include the position in which the assembly is located on an orbiting vehicle, the size of the spacecraft, or the potential use of thermal controls, including heaters.

Environments vary dramatically for different spacecraft (see Figure 16). The diurnal external environment encountered by Opportunity on the Martian surface has ranged from about –85°C to +21°C for a single Sol [19]. Opportunity is still operating accumulating 3744 Sols of mission time by August 5, 2014 [20]. In contrast, the internal computing environment of Landsat Data Continuity Mission, commissioned as Landsat-8 on May 30, 2013]21], has an approximate internal operating temperature range in one of the key instruments of about +25°C to +35 °C, including temperature rise due to power dissipation. This temperature range will be encountered with each 90 minute orbit over the 5 year mission life.

Figure 16. Opportunity rover (left) and Landsat-8 (right) representing a range of mission environments from planetary surface to low Earth orbit.

Test conditions selected for a specific system qualification should envelope the expected environment. Standard accelerated environments are useful in developing appropriate test conditions as indicated in this paper. Figure 14 shows several useful standards for mechanical test development. IPC 9701 is a useful document for selecting accelerated thermal cycling test conditions, given thermal cycling expected in use [22]. Test conditions for a sensor on the external elements of a rover may need a custom test environment. However, 0-100 °C may serve well as a test conditions for the internal computing environment of a LEO mission. It is important to note that increasing the level of acceleration often increases the complexity of estimating an acceleration factor and decreases the accuracy of interpretations of the test result. For soldered assemblies this is particularly true given the difficulties in the changing properties of the alloy and the creep component of the deformation [23].

Life Projection and Risk for Solder Joint Interconnections

As stated, the acceleration factor determinations are of prime importance in developing accelerated test designs. In the case of test conditions for solder joints in the range of 0-100°C, the Engelmaier modification of the Coffin-Manson fatigue relationship, shown in Table 1, may be useful for thermal cycling environments. For greater temperature ranges, the Norris-Lanzberg modification shown in Equation 3, can be conservatively used for some types of soldered structures, since larger thermal cycling temperature ranges were incorporated into the development of the Norris-Landzberg model [24, 25]. Strain energy models are also appropriate to large temperature ranges.

Following from equation 3, the derivation of an acceleration factor (AF) begins with the following expression comparing test and use conditions:

$$AF = \frac{N_{test}}{N_{use}} \qquad (4)$$

The life models shown in Table 1 can then be applied to determine the appropriate AF expression. In the case of the Engelmaier Model shown in Table 1, the AF expression becomes:

$$AF = \frac{\Delta T_{test}^{-1/c_{test}}}{\Delta T_{use}^{-1/c_{use}}} \qquad (5)$$

Where, c, accounts for creep:

$$c = -0.442 - 6x10^{-4}\bar{T} + 1.74x10^{-2}\ln\left[1 + \frac{360}{t_d}\right] \qquad (6)$$

In the above expressions, ΔT is the temperature range, $\bar{T}$ is the mean cycle temperature and t_d is the cyclic hold time [14]. Equations (4), (5) and (6) will be revisited in an example.

Qualification testing often cannot be run in a reasonable time duration to demonstrate actual desired reliabilities of devices. However, tests may be run to a set of risk preferences for a given project. Risk preferences for a given system design are held by the decision maker. However, these may be influenced by standardized organizational risk preferences. An example of risk likelihood classifications is shown in Table 2 for unmanned spacecraft.

Table 2. Risk Likelihood Classifications Used in GSFC-STD-0002 [26].

Likelihood	Safety (Estimated likelihood of safety event occurrence)	Technical (Estimated likelihood of not meeting performance requirements)
5 Very High	($P_{SE} > 10^{-1}$)	($P_T > 50\%$)
4 High	($10^{-2} < P_{SE} \leq 10^{-1}$)	($25\% < P_T \leq 50\%$)
3 Moderate	($10^{-3} < P_{SE} \leq 10^{-2}$)	($15\% < P_T \leq 25\%$)
2 Low	($10^{-4} < P_{SE} \leq 10^{-3}$)	($2\% < P_T \leq 15\%$)
1 Very Low	($P_{SE} \leq 10^{-4}$)	($0.1\% < P_T \leq 2\%$)

Using standardized risk preferences for qualification test design can inform quickly inform projects concerning the impact of using new and advanced packaging technologies. Risk preferences will also include the desired confidence limit for the qualification test. Risk criteria in the form of the desired probability of failure to be demonstrated, the confidence level desired can then be traded off against sample size and test time to provide for a test which meets schedule and cost constraints [27]. These parameters are traded off using equations (7) and (8).

$$1 - \mathbf{CL} = \sum_{k=0}^{r} \binom{n}{k} \left[1 - e^{\left(Ntest/\eta\right)^{\beta}}\right]^{k} \left[e^{\left(Ntest/\eta\right)^{\beta}}\right]^{n-k} \quad (7)$$

$$\eta = \frac{N_{Demo}}{(-\ln R(N)_{Demo})^{\frac{1}{\beta}}} \quad (8)$$

In the above model, known as Binomial Parametric test design [28], *CL*=confidence limit, *n*= number of samples, *r*=allowable failures, N_{test} is the number of cycles to be executed in test without acceleration, β=Weibull shape factor, N_{demo} is the desired number of cycles to be demonstrated on a component as used, $R(N)_{Demo}$ is the reliability of the component to be demonstrated in the test in, consideration of risk preferences, where R(N)= 1-F(N), given a preferred risk of failure to be below F(N).

In some cases, certain technologies can present variances or defects. In this case defects should be taken into consideration in test designs. Voids in solder joints are an example of a variance which has the potential to reduce the lifetime of an assembly in thermal cycling. Void defects for area array packages are defined in IPC 7095 [29]. In evaluating such defects with a RISQ, based qualification means such defect content as arising in the process must be represented within the qualification test articles.

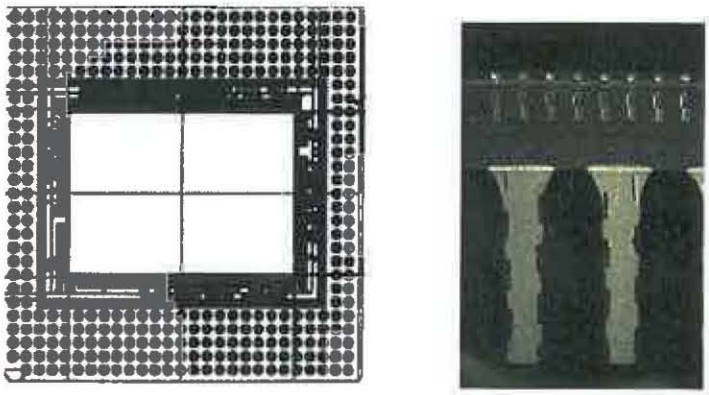

Figure 17. Device package for example RISQ analysis

Example of RiSQ for LEO Application

An example RISQ test design for a LEO mission advanced package is shown below. This example exercises the process shown in Figure 20. The system will be designed to meet a 5 year life. For a LEO orbit this will require the spacecraft to encounter 26816 diurnal cycles based on a 98 minute orbit. Power on cycles will be required with each orbit. The thermal analysis exercised on the system reflects a minimum temperature of 20°C on the cool side to the orbit reaching a maximum of 35°C on the hot side of the orbit with 5 watts dissipated by the devices. The system requires 3 fully function devices over the life of the spacecraft.

The type of device to be qualified is a 337 pin ASIC device employing a CGA package. The device outline and column configuration is shown in Figure 17. It is expected under small strains that lead stiffness will result in shear failure in the 63-37 SnPb attachment, similar to Figure 11.

In this example, the IPC 9701 test condition 1 (TC1) temperature ranges were selected with a 30 minute dwell time to more closely represent the on orbit conditions. The orbit and test conditions are summarized in Table 3.

Table 3. Test and Use Conditions of a LEO RISQ Analysis

Engelmaier Fatigue Exponent **Test**	**Values**
Average Temperature	50 °C
Cycle Hold Time	30 minutes
c_t	-0.43
$1/c_t$	-2.34
Engelmaier Fatigue Exponent **On Orbit**	
Average Temperature	30 °C
Cycle Hold Time	45 minutes
c_o	-0.42
$1/c_o$	-2.37
Orbit Conditions	
Min Temp On Orbit	20 °C
Max Temp on Orbit	35 °C
Temp Range on Orbit	15
Test Conditions	
Min Temp On Test	0
Max Temp on Test	100 °C
Temp Range on Test	100 °C
Test Acceleration Factor	**78**

The risk preferences for the test require that the loss of performance from an open circuit in the system be less than 0.1% for the three required devices in the circuit, at a confidence level of 95%. The individual device failure probability necessary for the test design, given three required devices can be estimated from the following:

$$R(Ndemo) = R_{sys}^{1/3} \qquad (9)$$

Equation (9) considers the devices to be in series in the system, with each device required to perform its functions. With a desired failure probability of 0.1% at the system level, each device will be re-

quired to have a required failure reliability to be demonstrated by the test, to be 0.03%, to meet the desired system risk preference for the devices.

Table 4 summarizes the results of the analysis. Given the results in Table 4, n=10 units can be assembled and run in test for 2500 cycles to meet the desired risk preference for the LEO systems, considering a whole device to be the item under test. Note that careful consideration must be given to selection of the Weibull shape parameter, β. Larger global strains tend to provide larger values of β, which may not be representative of actual use conditions [23].

Table 4. Trade off Study for Various Sample Sizes Given the Risk Preferences and Acceleration Factor from Table 3.

Failure Mode: Open Circuit				
Sample Size n	10	12	15	33
Allowed Failures , rf	0	0	0	0
Weibull Shape Parameter β	3.5	3.5	3.5	3.5
Confidence Level CL	0.95	0.95	0.95	0.95
Probability of Failure F(N)	0.03%	0.03%	0.03%	0.03%
Life on Orbit (Cycles)	26816	26816	26816	26816
Failure Free Test Time (No Acceleration)	192904	183113	171803	137150
Failure Free Test Time (Under Acceleration)	2473	2348	2203	1758

SUMMARY

This paper presented an overview of microelectronics packaging trends and roadmaps in a graphical style and description projected by the ITR Roadmap. The single-die packaging technologies with emphasis on ball grid array and column grid arrays were discussed in detail revealing the technologies that rapidly dominating packaging today. Accelerated reliability approaches under thermal and mechanical stresses for packages and assemblies were shown and are key to effective assessment of these technologies. Models that are necessary for projecting thermal cycle life from the thermal cycle testing were presented along with key accelerated thermal and mechanical reliability test specifications. These tools are useful for developing and designing accelerated test conditions and interpreting the results.

A unique analysis methodology that addresses risk from design to implementation, Risk Informed Systems Qualification, has been described. An example as how the RISQ analysis is used and how it has effectively addressed risk for a LEO spacecraft environment has been shown. Acceleration thermal and mechanical testing combined with risk informed systems qualification and analysis are key enablers for insertion of advanced microelectronics packages in various systems. These evaluations are aimed at providing a baseline for the industry and user community to better understand use of very dense and newly available advanced electronic packages including area array packages with known reliability and risks, allowing greater processing power in a smaller board footprint and lower system weight.

ACKNOWLEDGMENTS

The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration (NASA). Copyright 2014. All rights reserved.

Reza Ghaffarian would like to acknowledge various supports at JPL and NASA Headquarters, Office of Safety and Mission Assurance (OSMA). Furthermore, the authors extend their appreciation to program managers of the NASA Electronics Parts and Packaging (NEPP) Program,

including Michael Sampson, Ken Label, Dr. Charles Barnes, and Dr. Douglas Sheldon, for their continuous support and encouragement. Special thanks to Dr. Jean-Paul Clech and Dr. Jillian Y. Evans for their useful comments.

REFERENCES

[1] Ghaffarian, R., "Reliability of Column/Board CCGA Attachment," IEEE InterSociety Thermal Conference (ITherm), San Diego, CA May 31–June 2, 2012.

[2] Ghaffarian, R., "Assembly and Reliability of 1704 I/O FCBGA and FPBGA," in Proceedings of IPC/APEX, San Diego, CA, Feb.28–March 1, 2012.

[3] Ghaffarian, R. "Thermal Cycle and Vibration/Drop Reliability of Area Array Package Assemblies," Chapter 22 in Structural Dynamics of Electronics and Photonic Systems, eds. E. Suhir, E. Connally, and D. Steinberg (Wiley 2011).

[4] Ghaffarian, R., "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," IEEE Transactions on Components and Packaging Technologies, June 2008, Vol. 31, Issue 2.

[5] Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, ed. E. Suhir (Springer, 2006).

[6] Ghaffarian, R. "CCGA Packages for Space Applications," Microelectronics Reliability 46 (2006) 2006-2024.

[7] Tasooji, A., Ghaffarian, R., Rinaldi, A. "Design Parameters Influencing Reliability of CCGA Assembly and Sensitivity Analysis," Proceedings of ITherm, San Diego, CA (May 30-June 2, 2006.

[8] Ghaffarian, R., "Characterization and Failure Analyses of Lead-Free Solder Defects," Chapter 10 in Lead-Free Solder Interconnect Reliability Book, ed. D. Shangguan (ASM International, 2005

[9] Fjelstad, J., Ghaffarian, R., and Kim, Y.G., Chip Scale Packaging for Modern Electronics (Electrochemical Publications, 2002).

[10] Ghaffarian, R., "Chip Scale Package Assembly Reliability," Chapter 23 in Area Array Interconnection Handbook, Karl Puttlitz, Paul A. Totta, Kluwer (Academic Publishers, 2001)

[11] ITRS, International Technology Roadmap for Semiconductors, http://www.itrs.net/, accessed July 2014

[12] INEMI, International Electronics Manufacturing Initiatives, http://www.inemi.org/2013-roadmap, accessed July 2014

[13] IPC, Association Connecting Electronics Industry, http://www.ipc.org, accessed July, 2013

[14] Engelmaier, W., "Solder Joint Reliability, Accelerated Testing and Result Evaluation," chapter in Solder Joint Reliability: Theory and Applications, John Lau, ed., Van Nostrand Reinhold, New York, 1990.

[15] NEPP, NASA Electronics Parts and Packaging Program, https://nepp.nasa.gov/

[16] IPC, Association Connecting Electronics Industry, http://www.ipc.org/4.0_Knowledge/4.1_Standards/SpecTree.pdf., accessed July , 2014

[17] JEDEC, http://www.jedec.org/, accessed July, 2014

[18] DLA Land and Maritime, http://www.landandmaritime.dla.mil/Programs/MilSpec/DocSearch.aspx.. accessed July, 2014

[19] Spanovich, N. Smith, M.D. Smith, P.H. Wolff, M.J. Christensen, P.R. Squyres, S.W Surface and near-surface atmospheric temperatures for the Mars Exploration Rover landing sites, Icarus 180 (2006) 314–320.

[20 http://mars.jpl.nasa.gov/mer/gallery/all/opportunity.html

[21 http://www.nasa.gov/mission_pages/landsat/main

[22] IPC 9701, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, IPC, Chicago, IL, 2002.

[23] Evans, J.W., Kwon, D., Evans, J.Y., W. Engelmaier (edt.), A Guide to Pb Free Solders, Springer-Verlag, London, 2007.

[24] Norris, K.C. and Landzberg, Reliability of Controlled Collapse Interconnections, IBM Journal of Research and Development, Volume 13, Number 3, Page 266 (1969).

[25] Osterman, M., Effect of Temperature Cycling Parameters (Dwell and Mean Temperature) on the Durability of Pb-free solders, IMAPS Chesapeake-area Winter Technical Symposium, January 27, 2010.

[26] GSFC-STD-0002, Risk Management Reporting, May, 2009.

[27] Evans, J.W., Barto, A., Gallagher, B., Finley, P., Samuel, M. Burke, J., Analysis and Life testing for Design of Cryogenic Bearing Assemblies on the James Webb Space Telescope Optical Telescope Element, Proceedings of the ASME 2013 International Mechanical Engineering Congress & Exposition, IMECE2013, November 15-21, 2013, San Diego, California, USA

[28] Kececioglu, D., Reliability and Life Testing Handbook, Volume 1, Prentice hall, NJ, 1993.

[29] IPC 7095, Design and Assembly Process Implementation for BGAs, IPC, Chicago, IL, 2008.